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CVD MoS_2 for High Speed Devices and Circuits

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CVD MoS_2 for High Speed Devices and Circuits

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Dedication

To my parents Murlidhar and Sudha Sanne, and my siblings, Alka and Akshay Sanne, for all their love and support.

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CVD MoS_2 for High Speed Devices and Circuits

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ABSTRACT

Two-dimensional layered materials (2DLMs) have been widely studied as a potential alternative to the complementary metal-oxide semiconducting field-effect transistor (CMOS FET) "switch." The atomically thin body of 2DLMs lends itself to improved electrostatic gate control, leading to a suppression of the short channel effects which limit the scalability of CMOS devices. While many experiments have examined 2DLMs as a low power solution for aggressively scaled digital devices, their feasibility study for use in high speed radio frequency (RF) devices and circuits is still in its infancy. Current technological trends such as the Internet of Things (IoT) and 5G communication have increased the demand for novel high speed devices to serve next-generation circuits and systems.

Graphene, as a 2DLM, has garnered significant interest for its use in high speed radio frequency (RF) devices and circuits. A carrier mobility greater than 10,000 cm^2/Vs, ambipolar transport, and excellent thermomechanical stability has afforded graphene cutoff frequencies greater than 400 GHz. Multi-transistor integrated circuits, including a fully integrated RF receiver have been demonstrated using graphene. However, graphene poses a limitation in high speed operation in that the Dirac cone band structure results in a zero

bandgap, leading to semi-metallic transport behavior. As a result, graphene field-effect transistors (GFETs) exhibit a low I_{ON}/I_{OFF} ratio and non-saturating output behavior. This translates to FETs showing reduced power and voltage gains, hindering the realization of high performance amplifiers, mixers, and other RF circuit elements.

Another class of 2DLMs has generated renewed interest for its potential to replace silicon as the next-generation CMOS "switch." Transition metal dichalcogenides (TMDs) is a family of 2DLMs with the general chemical formula MX_2 (M = metal, X = chalcogen). Of the class of TMDs, molybdenum disulfide (MoS_2) is of special interest. With its thickness-dependent electronic properties, MoS_2 has been considered for applications in the fields of opto-electronics, flexible electronics, spintronics, and coupled electro-mechanics. Its single layer direct bandgap of ~1.8 eV allows for high I_{ON}/I_{OFF} metal-oxide semiconducting FETs. More relevant for RF applications, theoretical studies predict MoS_2 can afford saturation velocities, v_{sat}, greater than 3×10^6 cm/s. While the mobility of MoS_2 is lower than that of graphene, the intrinsic bandgap in MoS_2 has shown voltage gains, $A_v = g_m/g_{ds}$, greater than 30. Thus far, most of the studies of graphene and MoS_2 have utilized crystalline exfoliated layers, which provide a convenient high quality source of material for laboratory experiments. However, for industrial scale applications, the mechanical cleavage process is not scalable and, thus far, there have been few studies on large area chemical vapor deposited (CVD) MoS_2 RF FETs. In this dissertation, the initial efforts to utilize CVD MoS_2 for RF FETs are presented. The RF figures-of-merit transit frequency, f_T, and maximum frequency of oscillation, f_{max}, are measured for CVD MoS_2. The effects of different substrates and superstrates on MoS_2 are investigated. In order to improve the cutoff frequencies, a combination of channel length scaling and device geometry modifications are applied. Simple RF circuits are demonstrated experimentally using CVD MoS_2 FETs. Additionally larger circuit building blocks are simulated using experimental

data. The goal of this work is to provide a baseline of the RF performance achievable using CVD MoS_2. Hopefully, this work will motivate future studies directing MoS_2 towards industrial electronic applications.

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CHAPTER 1: The Effects of Substrates and Superstrates upon Two-Dimensional Layered Materials

1.1.1 INTRODUCTION

The effects of the substrate and superstrate upon two-dimensional layered materials (2DLMs) can greatly affect both the carrier contact injection and transport through the channel material. This is because confinement of charge carriers to a 2D plane amplifies the effects of the surrounding environment. Here the various effects of the substrate and superstrate upon single layer graphene and molybdenum disulfide (MoS_2) are examined, which in turn can be extended to general 2DLMs. The initial discovery of single layer graphene from the now famous "scotch tape" method served as a precursor for one of the most advantageous aspects of 2DLMs [1]. This is the ability to "pick-up" a particular 2D layered sheet and transfer it upon a target substrate of choice. This has opened up many experimental avenues, such as the stacking of different "flavors" of 2DLMs to examine the physics of the interlayer interactions. A highly insulating substrate such as sapphire or Al_2O_3 could serve as an ideal substrate for high frequency operation. Additionally one may even transfer 2DLMs upon flexible substrates to unlock the "bendability" of the ultrathin layers.

The results reported in this chapter have been published in: (1) "Poly (methyl methacrylate) as a self-assembled gate dielectric for graphene field-effect transistors" by A. Sanne, H. C. P. Movva, S. Kang, C. McClellan, C. M. Corbet, and S. K. Banerjee in Applied Physics Letters, vol. 104, issue 8, pp. 083106, (2014). Contributions: A. Sanne and H. C. P. Movva carried out the device design, fabrication, and electrical characterization with contributions from S. Kang, C. McClellan, and C. M. Corbet. S. K. Banerjee supervised the work, and all authors reviewed and commented on the results and the manuscript. (2) "Top-gated chemical vapor deposited MoS_2 field-effect transistors on Si_3N_4 substrates" by A. Sanne, R. Ghosh, A. Rai, H. C. P. Movva, A. Sharma, R. Rao, L. Mathew, and S. K. Banerjee in Applied Physics Letters, vol. 106, issue 6, pp. 062101, (2015). Contributions: A. Sanne carried out the device fabrication. A. Sanne, A. Rai, and H. C. P. Movva contributed to the electrical characterization. A. Sharma and R. Ghosh performed the material growth. R. Rao, L. Mathew, and S. K. Banerjee supervised the work, and all authors reviewed and commented on the results and the manuscript. A. Sanne is the corresponding author for the publications.

Ideal crystallographic graphene has a chemically inert surface without the dangling bonds needed for nucleation sites in atomic layer deposition (ALD) steps. As a result hexagonal boron nitride (hBN) has been shown to be an excellent encapsulating layer as the two materials share the same hexagonal crystal structure. But beyond lattice matching, the chemical composition of the encapsulating interface can cause severe carrier fluctuation in the graphene layer. This has been shown to be true on graphene on several substrates including SiO_2, HfO_2, Al_2O_3 and Si_3N_4 [2]. The most common technique to nucleate the graphene surface is to deposit a thin metallic layer, and then allow the ambient environment to partially oxidize the surface. However, this has a negative effect on the mobility as it increases the long range and short range scattering parameters [3, 4]. The ideal gate dielectric for a graphene FET avoids the need for a nucleation layer, is scalable, and does not disrupt the charge neutrality point.

MoS_2, similar to graphene, is also highly sensitive to the underlying substrate and superstrate. Multi-layer MoS_2 back-gated FETs on 50 nm Al_2O_3 substrates have shown back-gated mobilities > 100 cm^2/Vs [5], while multilayer MoS_2 FETs on 50 nm thick spin-coated poly(methyl methacrylate) (PMMA) substrates have achieved back-gated mobilities > 400 cm^2/Vs [6]. Furthermore, the mobility can be engineered by applying an appropriate top gate dielectric, such as HfO_2, Al_2O_3, or polymer dielectrics [6, 7, 8]. Applying a high-*k* dielectric as either a substrate or superstrate increases the screening of charged impurities in the MoS_2 layer, which may enhance the mobility [9]. The interfacial-oxygen-vacancy mediated doping of MoS_2 by high-*k* dielectrics, in general, leads to improved screening of charged impurities, suppression of homopolar phonon scattering, and reduction of the effective Schottky barriers at the contacts The substrate may affect FET performance by introducing long range or short range charge disorder. It has been shown that the MoS_2

follows the morphology of the substrate surface, whereby a rough surface may affect long range and short range scattering parameters.

1.2 GRAPHENE FETS WITH PMMA AS A GATE DIELECTRIC

Most graphene field effect transistor (GFET) gate dielectric studies have focused on high-*k* dielectrics such as HfO_2 and Al_2O_3, for reasons similar to those for Si CMOS, such as high transconductance. Many of the high-*k* dielectric deposition processes, for instance, by ALD, require a "seed layer" to nucleate the dielectric film due to the intrinsic chemical inertness of the graphene surface. Low-*k* dielectrics are used in conventional Si CMOS in the back-end to reduced RC time constants of metal interconnects.

One common low-*k* dielectric commonly used in the fabrication process of 2DLMs is poly(methyl methacrylate) (PMMA). It is mainly used for lithographic patterning steps as a positive mask in electron beam lithography (EBL). Often PMMA residues are retained on the surface of 2D materials in the course of the fabrication process. Typically this is undesirable it serves as a p-type dopant shifting the graphene Dirac point to more positive voltages. Additionally GFETs with PMMA residues suffer mobility reductions. Additional annealing steps can be performed to remove these residues, but this increases the overall thermal budget of the GETs. An alternative approach to this problem is to retain the PMMA residues and exploit them as a low-*k* self-contained organic gate dielectric for graphene field effect-transistors (GFETs). The use of PMMA as a gate dielectric avoids ALD-type steps for a low thermal budget process solution. Initial device trials proved that high temperature baking steps above the glass transition temperature (~130 ºC) can leave a self-assembled, thin PMMA film on graphene, where a gate dielectric is created without additional atomic layer deposition type steps [10].

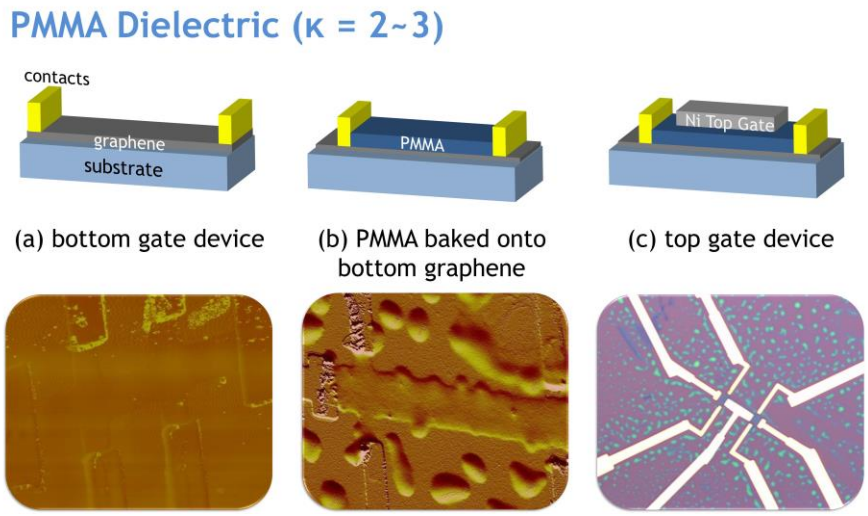

Figure 1.1: (top) Process flow for a dual-gated GFET with a PMMA gate dielectric. The substrate is used as the back gate. For 4 point measurements, there are additional Hall probes within the contacts. (bottom) AFM and optical microscope images of the corresponding device in the process flow. The bottom-left image is an AFM image of a typical GFET with a clean surface. The bottom-middle image is an AFM of the GFET with PMMA residues prior to top-gate deposition. The PMMA film is approximately 8nm thick. The bottom-right image is an optical micrograph of a dual-gated GFET with a PMMA gate dielectric. The scale bars in all images are 1 μm.

Dual-gated GFETs are fabricated as follows. The graphene active region is defined by e-beam lithography, and the excess graphene is etched away using O_2 plasma. Next, metal contacts are defined by a second e-beam lithography step. Nickel is deposited as a source/drain contact metal using e-beam evaporation. A pre-liftoff high temperature bake is done to ensure that there are PMMA residues. The samples are then soaked in acetone. The acetone removes all the PMMA except a thin surface layer on the graphene. Next, back-gated electrical measurements of the GFETs are taken. A second, longer PMMA cure well above the PMMA glass transition temperature is done to further improve dielectric uniformity. The top gate is then defined by e-beam lithography and a Ni gate electrode is deposited. Figure 1.1 is an outline of the process flow for a GFET with a PMMA gate dielectric. Figures 1.1(a) and 1(b) are atomic force microscope (AFM) images of the GFET

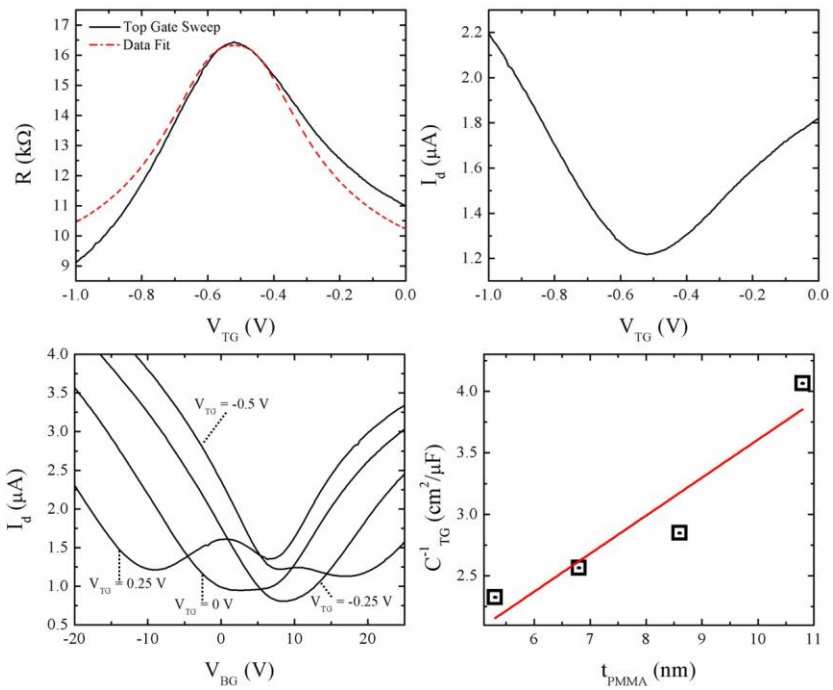

Figure 1.2: (a) Resistance, R, vs. top-gate voltage, V_{TG}, measured in a dual-gated GFET with a PMMA dielectric. The curve is fit using a single mobility fit. The mobility of this device is 9600 cm^2/Vs. (b) Drain current, I_d, vs. V_{TG}. (c) I_d vs. back gate voltage, V_{BG}, for different V_{TG}. (d) $V_{Dirac,BG}$ vs. V_{TG} measured from the R vs. V_{BG} traces for different top-gate biases.

channel before and after the PMMA baking step. Figure 1(c) is an optical microscope image of the dual-gated GFET.

Figure 1.2(a) shows a dual-gated GFET channel resistance measured as a function of the top-gate voltage (V_{TG}). The electrical measurements were taken using 4-point resistance method, with a drain bias of 20 mV. The top-gate is insulated with 8 nm of PMMA measured with step height profiles using AFM. The resistance curve is fit using a simple GFET mobility model [11], and the estimated mobility is 9600 cm^2/Vs. Figure 1.2(b) is the drain current (I_d) as a function of top-gate modulation. Figure 1.2(c) is the drain current as a function of the back gate voltage (V_{BG}) at different V_{TG} voltages. Each trace shows the ambipolar characteristic of GFETs, with two charge neutrality points. This is because the GFETs have a middle channel region that is dual-gated and source-drain

access regions that are bottom-gated. The bottom-gated access region exhibits a fixed Dirac point at 9.7 V while the top-gate dependent Dirac point shifts with top-gate bias. The V_{BG} value at the charge neutrality point ($V_{Dirac,BG}$) has a linear dependence on V_{TG}, as shown in Figure 1.2(c). The slope of the $V_{Dirac,TG}$ vs. V_{BG} data is the ratio of the back-gate capacitance (C_{BG}) to top-gate capacitance (C_{TG}). The bottom dielectric capacitance is measured using 100 x l00 μm^2 metal pads deposited on SiO_2 to have a value of 8 $nF/\mu m^2$. Using the measured C_{BG}/C_{TG} ratio and the measured value of C_{BG}, the value of C_{TG} is calculated for each dual-gated GFET. The quantum capacitance does not contribute to the measured C_{TG} because the C_{BG}/C_{TG} is determined from the dependence of the charge neutrality point on V_{BG} and V_{TG}, where the Fermi energy is zero. The top-gate capacitance is calculated and, from it, a PMMA gate dielectric constant $k = 3$ is extracted, which agrees well with reported values.

In summary, PMMA was found to be a viable low-*k* organic dielectric for GFETs. The PMMA gate dielectric can be formed almost for "free" as a by-product of the e-beam lithography process and high temperature bakes through the fabrication process.

1.3 CVD MoS_2 Substrate and Superstrate Effects

A large roadblock to potential graphene-based CMOS devices is the absence of a bandgap, due to graphene's Dirac cone band structure. As a result, other two-dimensional (2D) materials such as transition-metal dichalcogenides (TMDs) are being studied. Of the TMDs, MoS_2 has particularly attracted a lot of attention. MoS_2 is a 2D semiconductor with a bulk indirect bandgap of 1.3 eV, and a direct bandgap of 1.8 eV for single layers [12, 13, 14]. Its bandgap allows for high I_{ON}/I_{OFF} metal-oxide semiconducting field-effect transistors (MOSFETs). Top-gated FETs based on exfoliated monolayer MoS_2 flakes on

SiO_2 have shown room temperature mobilities > 80 cm^2/Vs, with I_{ON}/I_{OFF} ratios exceeding 10^8 [15]. Multi-layer MoS_2 back-gated FETs on 50 nm Al_2O_3 substrates have shown back-gated mobilities > 100 cm^2/Vs, while multilayer MoS_2 FETs on 50 nm thick spin-coated PMMA substrates have achieved back-gated mobilities > 400 cm^2/Vs [3]. However, exfoliated MoS_2 flakes are typically small and cannot be scaled to large areas. One approach to obtaining large area MoS_2 is a chemical vapor deposition (CVD) growth process. Large area high quality films are necessary to move from laboratory experiments to industrial-scale production. This section examines substrate and superstrate effects on CVD MoS_2 as the initial step to evaluating MoS_2 FETs for digital and analog electronics.

Top-gated MoS_2 FETs were fabricated as follows. Suitable CVD-grown MoS_2 flakes were identified using a combination of optical contrast, Raman spectroscopy, and AFM images. Device active regions were defined using e-beam lithography. Excess MoS_2 was etched using Cl_2 plasma. Next, metal electrodes were defined with a second e-beam lithography step. A stack of silver/gold (20 nm/30 nm Ag/Au) was deposited as a low-work function (4.26 eV) source/drain metal electrodes to enhance n-type conduction of the MoS_2 FET. Following a metal liftoff in acetone, ALD was used to deposit a 25 nm thick layer of Al_2O_3 or HfO_2 as a top-gate dielectric. The top-gate electrode was then defined using a final e-beam lithography step and deposited as a 50 nm stack of Ni/Au. A final metal liftoff in acetone completed device fabrication. An optical image of the final device structure used for temperature dependence and mobility extraction is shown in the inset of Figure 1.3(b).

Figure 1.3(a) is the I_{ds}-V_{gs} transfer characteristics of a CVD MoS_2 transistor with a top-gate dielectric of Al_2O_3. For all DC measurements, the device gate length (L_g) is 300 nm and the widths (W) vary from 10 µm to 25 µm, depending on the size of the CVD MoS_2 domain. The top gate voltage (V_{tg}) is swept from -7 V to 7 V with the drain voltage (V_{ds}) varying from 0.1 V to 2 V. The device exhibits a threshold voltage (V_{th}) around -4 V,

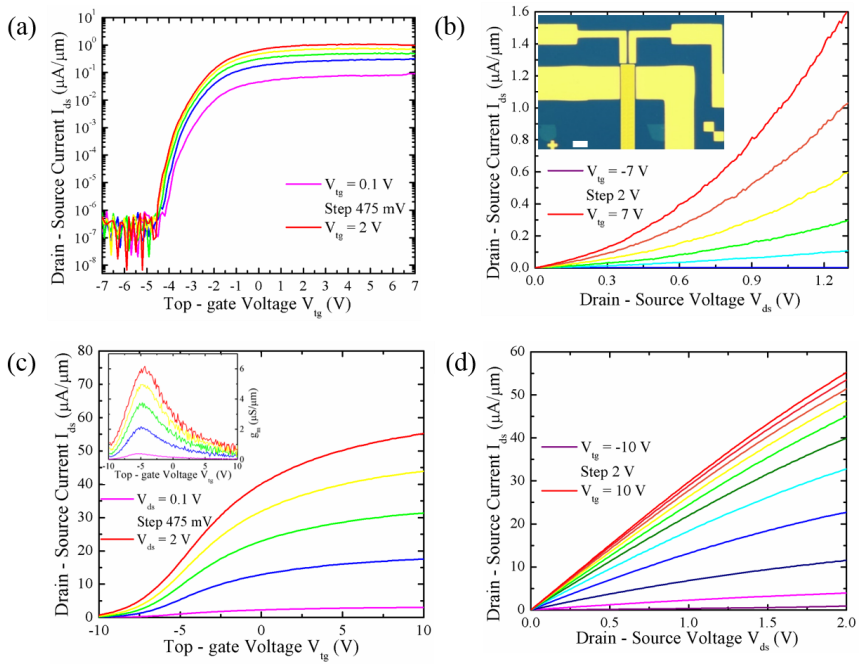

Figure 1.3: (a) Drain-to-source current, I_{ds}, vs. top-gate voltage, V_{tg}, for different drain voltages, V_{ds}, on an Al_2O_3 top-gated device. The threshold voltage, V_{th}, is around -4 V indicating n-type doping of the MoS_2. The I_{ON}/I_{OFF} ratio reaches 10^7 at a V_{ds} of 2 V. (b) Drain-to-source current, I_{ds}, vs. drain voltage V_{ds} for different V_{tg}. The device shows negligible currents until a V_{tg} of -2 V. Inset: Optical image of a top-gated MoS_2 FET. (c) Drain-to-source current I_{ds} vs. top gate voltage V_{tg} for different drain voltages V_{ds} on an HfO_2 top-gated device. Inset: Transconductance g_m vs. top gate voltage V_{tg}. (d) Drain-to-source current I_{ds} vs. drain voltage V_{ds} for a HfO_2 top-gated device. With HfO_2 as a gate dielectric, current drives are much larger and saturation is improved. The scale bar is 5 μm.

indicating n-type doping of the MoS_2, extrinsically during fabrication or intrinsically during growth. This is common for both CVD and exfoliated MoS_2 devices, intrinsically caused by sulfur vacancies in the MoS_2 and extrinsically by doping sources such as PMMA and acetone. With Al_2O_3 as the top gate dielectric, the I_{ON}/I_{OFF} ratios exceed 10^7 at a V_{ds} of 2 V with off-state currents less than 10^{-7} μA/μm. Using the slope of the I_{ds}-V_{gs} curve in the linear region, the field-effect mobility is calculated using $\mu_{FE} = \left[\frac{dI_{ds}}{dV_{gs}}\right]\left[\frac{L}{WC_{ox}V_{ds}}\right]$. Operating at a low-field V_{ds} of 100 mV, a maximum mobility of 24 cm^2/Vs is extracted. Figure 1.3(b) shows the I_{ds}-V_{ds} output curves. The non-linear concave-up curves indicate a

significant Schottky barrier to transport. Figure 1.3(c) is the I_{ds}-V_{gs} transfer characteristics and Figure 1.3(d) is the I_{ds}-V_{ds} output characteristics of a monolayer CVD MoS_2 transistor with a top gate dielectric of HfO_2. The current densities for HfO_2 are much larger than that of Al_2O_3, exceeding 55 µA/µm at a V_{ds} of 2 V. As shown in the inset of Figure 1.3(c), the devices with a HfO_2 gate dielectric on Si_3N_4 substrates achieve a maximum transconductance (g_m) of 6 µS/µm at a V_{ds} of 2 V. The low Vds current shows greater linearity in HfO_2 compared to Al_2O_3, indicating a lowered Schottky barrier. This can be explained as a thinning of the contact Schottky barriers due to interfacial oxygen-vacancy mediated charge transfer doping. However, HfO_2 significantly degrades the I_{ON}/I_{OFF} ratio and induces a large negative V_{th} shift. This doping effect can be further confirmed by using HfO2 as both the substrate and superstrate. Figure 1.4 compares the transfer characteristics of a $SiO_2/MoS_2/HfO_2$ FET with a $HfO_2/MoS_2/HfO_2$ FET. The doping effects are further exaggerated in the HfO_2-sandwiched device. The V_{th} is now shifted negative beyond -10

V. The additional oxygen-deficient HfO_2 layer provides even more surface charge transfer doping to further improve current density. The choice between HfO_2 and Al_2O_3 presents a tradeoff between V_{th} shifts and I_{ON}/I_{OFF} ratios with current drive and transconductance. This tradeoff is further examined and utilized in the context of radio frequency (RF) devices in successive chapters.

1.4 SUMMARY

In summary, PMMA was found to be a viable low-k organic dielectric for GFETs. The PMMA gate dielectric can be formed almost for "free" as a by-product of the e-beam lithography process and high temperature bakes through the fabrication process. Measuring the inverse top-gate capacitance as the PMMA is scaled down, we measure the dielectric constant of PMMA to be around $k = 3$, which agrees with reported values. The dielectric constant is smaller for thinner dielectrics, possibly due to decreased polarization with

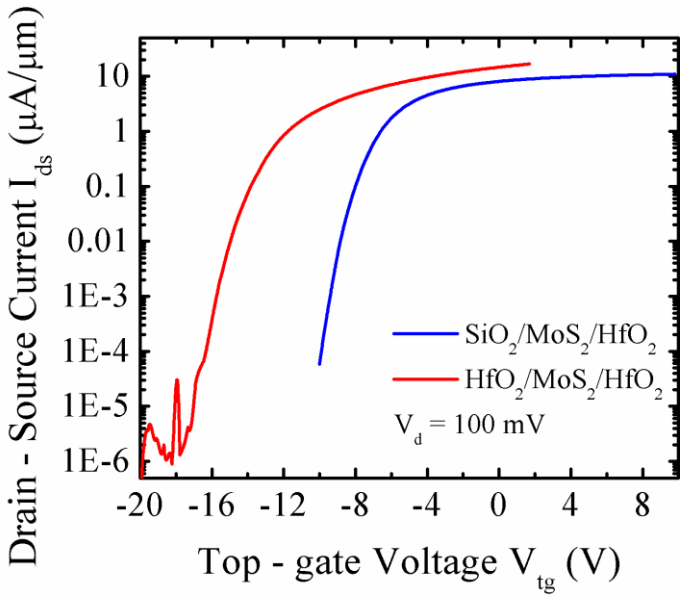

Figure 1.4: (a) Drain-to-source current I_{ds} vs. top-gate voltage V_{tg} for a MoS_2 HfO_2 top-gated FET compared with an HfO_2-sandwiched FET. The negative V_{th} shift is exacerbated in the sandwiched FET. The additional HfO_2 layer provides even more surface charge transfer to further improve current densities.

increased annealing budgets. The a low gate leakage current density of less than a $pA/\mu m^2$ and high channel mobilities of ~10,000 $cm^2/V\text{-}s$ can be achieved with this simple, low-*k* organic gate dielectric process.

Top-gated CVD MoS_2 FETs on Si_3N_4 show comparable electrical performance to SiO_2 substrates. We achieve a mobility of 24 cm^2/Vs with I_{ON}/I_{OFF} ratios exceeding 10^7. Using HfO_2 as a top gate dielectric, devices achieve current densities of 55 µA/µm and a transconductance of 6 µS/µm. Temperature dependence of mobility in MoS_2 on Si_3N_4 shows a strong suppression of charged impurity scattering and a weaker than expected dependence on phonon scattering, suggesting the Si_3N_4 may play a role in screening remote phonons.

CHAPTER 2: Top-gated CVD MoS_2 FETs Operating at Gigahertz Frequencies

2.1 INTRODUCTION

Using high-*k* dielectrics and substrate/superstrate engineering exfoliated monolayer MoS_2 FETs have shown $I_{ON}/I_{OFF} > 10^8$ with mobilities exceeding 80 cm^2/Vs [15]. Additionally, exfoliated monolayer MoS_2 FETs have exhibited current saturation with on-state current densities of 300 µA/µm, as well as transconductance exceeding 40 µS/µm. While the mobility of MoS_2 is lower than graphene, the intrinsic bandgap in MoS_2 has resulted in voltage gain, $A_v = g_m/g_{ds}$, greater than 30 [16]. Moreover, theoretical calculations predict electron saturation velocities greater than 3×10^6 cm/s [17], which is sufficient to afford GHz transit frequencies at sub-micron channel lengths. These properties make MoS_2 a desirable candidate for RF applications. Initial work on exfoliated monolayer MoS_2 RF FETs yielded an f_T of 2 GHz and f_{max} of 2.2 GHz at a gate length of 240 nm [14], while multilayer flakes have achieved an f_T of 42 GHz and f_{max} of 50 GHz at a gate length of 68 nm [16].

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A previous study on chemical vapor deposited (CVD) MoS_2 presented high frequency measurements and achieved an f_T of 900 MHz and f_{max} of 1 GHz at a gate length of 300 nm [18]. Simulations predict that much higher cutoff frequencies are possible as MoS_2 transistor channel lengths are scaled down to gate lengths of ~ 15 nm [19]. A wide array of both analog and digital electronic circuits based on MoS_2 have been demonstrated [20, 21]. Similar to the initial work done on graphene, most device characterizations using MoS_2 have utilized exfoliated samples. However, in order for MoS_2 based devices to move from laboratory studies to industrial scale applications, large area growth of high quality material is needed. Different methods including liquid exfoliation [22] and direct sulfurization of molybdenum thin films [23] have been successfully used to synthesize large MoS_2 monolayers. However, the overall simplicity and the high quality of films obtained using the sulfurization of MoO_3 has made it the most widely used method of synthesizing monolayer MoS_2 [24-26]. In this letter, we demonstrate high performance RF FETs based on CVD monolayer MoS_2 using the sulfurization of MoO_3. With operating frequency in the GHz range, we are able to realize amplifiers and frequency mixers with fabricated CVD MoS_2 FETs.

2.2 CVD MoS_2 Material Synthesis

Similar to the initial work done on graphene, most device characterizations using MoS_2 have utilized exfoliated samples. However, in order for MoS_2 based devices to move from laboratory studies to industrial scale applications, large area growth of high quality

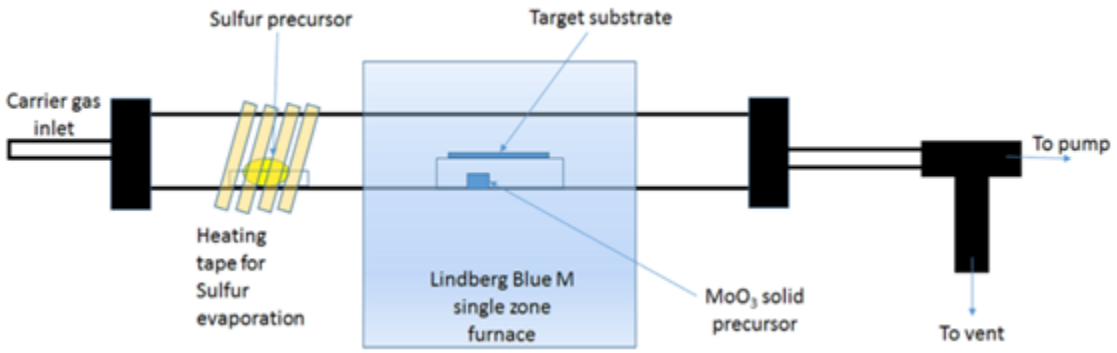

Figure 2.1: Schematic of the MoS_2 growth setup starting from the solid precursors MoO_3 and sulfur. The furnace was single zone, with independent heating sources for the MoO_3 and the sulfur sources.

material is needed. Different methods including liquid exfoliation and direct sulfurization of molybdenum thin films have been successfully used to synthesize large MoS_2 monolayers. However, the overall simplicity and the high quality of films obtained using the sulfurization of MoO_3 has made it the most widely used method of synthesizing monolayer MoS_2. As a result we chose the sulfurization of MoO_3 for synthesizing the large area MoS_2 used for all the device results presented here.

The MoS_2 atomic layer films were grown by a standard vapor transfer growth process (Figure 2.1) within a quartz tube with an inner diameter of 22 mm and a Lindberg/Blue M furnace. The starting materials were MoO_3 (15 mg) and sulfur (1 g)

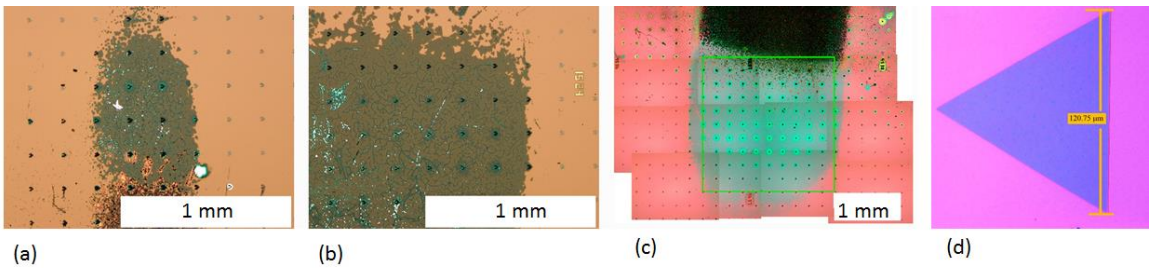

Figure 2.2: (a,b,c) Controlled large-area growth of continuous monolayer MoS_2 in the mm^2 scale. (d) Individual isolated domains with edge lengths > 100 µm.

powder that were loaded in separate alumina crucibles and placed inside the tube, with the sulfur crucible outside the actual furnace and heated independently using a heating tape. The substrates used for this work were surface cleaned 285 nm SiO_2 on highly resistive Si (> 5000 Ω·cm). Controlled large area growth was accomplished by using masking and target substrates. Both the masking and target substrates used were from the same wafer. The polished side of the substrates faced the MoO_3 precursor. By controlling the distance between individual masking substrates we could control the area of the continuous monolayer region. The procedure for the growth consisted of loading the starting materials and substrates, followed by pumping down the tube to base pressure (< 10 mTorr). This was followed by purging the tube and the gas lines by flowing in UHP N_2 gas at 200 sccm. After 4 purging cycles the tube was filled with N_2 to 1 atmosphere of pressure. Then the temperature of the furnace was raised to 850 °C at a rate of 50 °C/min. When the temperature of the tube furnace was at 650 °C, the sulfur was heated to 150 °C (+/- 5 °C) and held there at that temperature. The growth continued for 5 min at 850 °C. After the 5 minutes at 850 °C the heater in the furnace was turned off for cooling without any feedback. Heating of the sulfur was cut off once the furnace cooled down to 650 °C. Figure 2.2(a,b,c) show optical images of resulting large area growths. Figure 2.2(d) shows a typical individual triangular domain with an edge length of 100 μm to be used for device fabrication.

2.2.1 CVD MoS_2 Material Characterization

After the CVD MoS_2 material growth, it is necessary to evaluate the film quality. The film quality plays a large role in the electrical performance of the MoS_2 FET. Since the chemical vapor deposited MoS_2 was grown directly onto the SiO_2 surface used for device fabrication, we can directly measure the MoS_2 material with any additional transfer

steps. The advantage of this as compared to transferred films is we avoid any organic contaminants gathered during the transfer. As shown in Figure 2.3, thickness and material quality of the films were characterized using a combination of Raman spectroscopy, photoluminescence spectroscopy (PL), and transmission electron microscopy (TEM).

From the Raman spectrum in Figure 2.3(a), the E^1_{2g} peak is at 383.5 cm^{-1} and the A_{1g} peak at 403.1 cm^{-1}. This corresponds to a delta (Δ) of 19.6 cm^{-1}, which is characteristic of CVD grown monolayer MoS_2 [27]. The full width at half maximum (FWHM) of the E^1_{2g} and A_{1g} peaks is an indicator of the material quality of the film [28]. From the Raman spectrum,

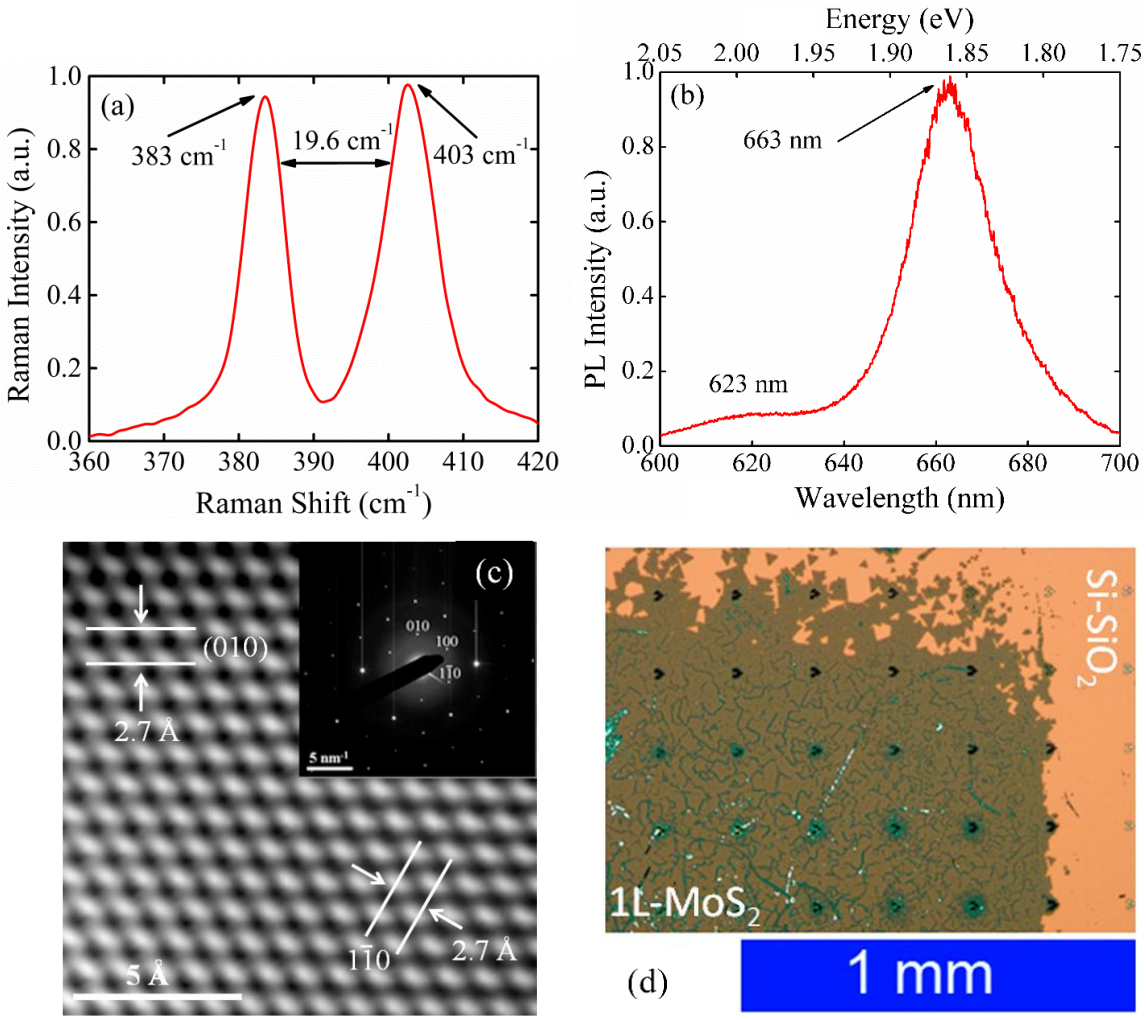

Figure 2.3: (a) Raman spectra of CVD MoS_2. The E_{12g} peak is at 383.5 cm-1 and the A_{1g} at 403.1 cm-1, corresponding to a delta of 19.6 cm-1. (b) Photoluminescence spectra of CVD MoS_2. There is a peak at 663 nm (1.87 eV) and a smaller peak at 623 nm (1.99 eV) corresponding to the A and B excitons. (c) FFT corrected high resolution TEM image of monolayer CVD MoS_2 with lattice spacing of 0.27 nm. The inset shows the diffraction pattern from the same area. (d) Large area MoS_2 growth in the mm^2 scale.

we measure a FWHM of 4.6 cm^{-1} for the E^1_{2g} peak and 5.9 cm^{-1} for the A_{1g} peak, which is similar to that reported for other CVD grown MoS_2 samples [29]. The strong signal obtained from the PL spectroscopy in Figure 2.3(b) further confirms the existence of a direct band gap that is expected in monolayer MoS_2. The strong peak around 663 nm (1.87 eV) and a much smaller peak around 623 nm (1.99 eV) correspond to the A and B excitons and is similar to those observed for exfoliated monolayer MoS_2 [30]. Transmission electron microscopy (TEM) was used in order to evaluate the crystallinity of the CVD MoS_2. Figure 2.3(c) shows the FFT filtered high resolution TEM image of monolayer MoS_2, while the inset shows the selected area electron diffraction (SAED) of the same region. The hexagonal lattice structure and the lattice spacing of 0.27 nm is as expected from crystalline MoS_2. Figure 2.3(d) shows mm-scale growth of single layer CVD MoS_2 on a SiO_2/Si substrate. Raman and PL spectroscopy was done using a Witec Alpha 300 micro-Raman confocal microscope, with the laser operating at a wavelength of 488 nm. Parameters in our mapping were (i) grating (Raman) = 1800 g/mm, (PL) = 600 g/mm; (ii) integration time/pixel = 1 s; (iii) resolution = 3 pixels/μm. TEM was done using a JEOL 2010F Transmission Electron Microscope.

2.3 TOP-GATED CVD MoS_2 RF FETS FABRICATION

Top-gated CVD MoS_2 FETs in the ground-signal-ground (GSG) layout for high-frequency characterization were fabricated as follows. Monolayer MoS_2 domains grown on highly resistive Si/SiO_2 substrates were identified using a combination of optical

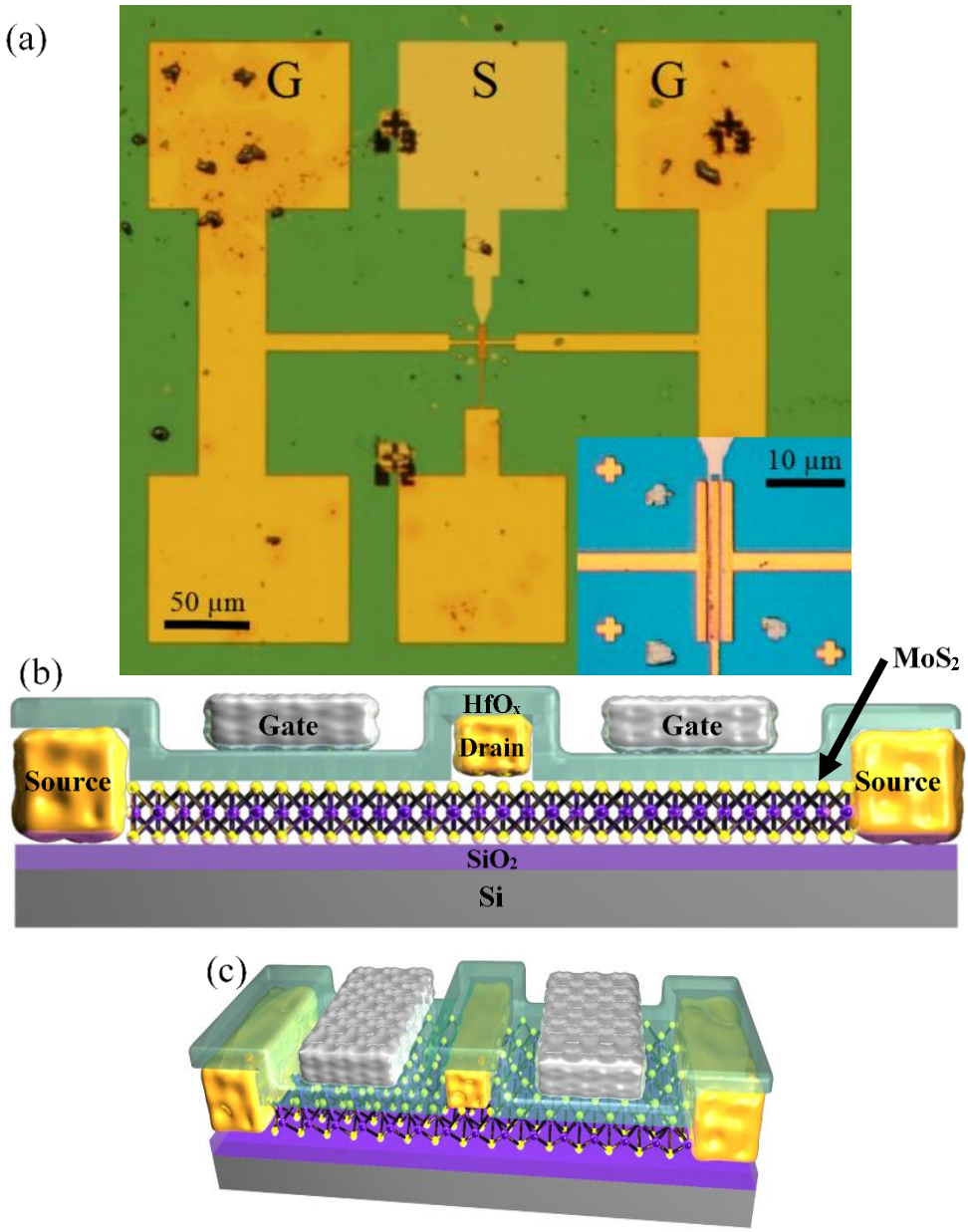

Figure 2.4: (a) Optical image of a CVD MoS_2 FET in the ground-signal-ground structure (GSG) required for high frequency measurements. The inset shows a zoomed in layout of a device with L_g = 250 nm and W = 20 µm. (b) Cross-sectional view of the MoS_2 transistor highlighting the underlap regions used to eliminate parasitic capacitances. The SiO_2 layer is 285 nm thick and the HfO_x is 30 nm thick. (c) 3D cartoon of a GSG MoS_2 FET.

contrast, Raman spectroscopy, and atomic force microscopy (AFM). Device active regions were defined using electron beam lithography (EBL). Excess MoS_2 was etched using Cl_2

plasma. Next, source/drain metal electrodes were defined with EBL. A stack of Ag/Au (20 nm/30 nm) was deposited as low-work function (4.26 eV) source/drain metal electrodes. It has been shown that as-deposited Ag films on MoS_2 results in a smooth and dense interface, thereby, facilitating electron injection in the MoS_2 channel [31]. Atomic layer deposition (ALD) was used to deposit a 30 nm thick layer of HfO_x with dielectric constant $k \sim 18$ as the top gate dielectric. The subscript "x" for the oxygen content represents the uncertain stoichiometry of the ALD hafnium oxide film. The top gate electrode was then defined using a final EBL step. The top gate metal fingers were formed with 50 nm of Ni. Figure 2.4(a) shows an optical image of the final device structure in the GSG configuration. Figure 2.4(b) shows a cross-sectional schematic of the GSG MoS_2 FET. Figure 2.4(c) is a 3D cartoon of a GSG MoS_2 FET. The gate length (L_g) of all devices was 250 nm, and was verified using AFM after device fabrication. Underlap regions of 100 nm were left on either side of the gate to prevent parasitic source/drain capacitances. However, these access regions add to the overall contact resistance of the device. Measurements presented were taken in ambient atmosphere at room temperature in the dark.

2.4 TOP-GATED CVD MoS_2 FETS DC CHARACTERIZATION

Figure 2.5(a,b) shows the I_{ds}-V_{gs} transfer characteristics and I_{ds}-V_{ds} output characteristics of a monolayer MoS_2 FET with a width, W, of 20 µm. The device achieves current densities of 200 µA/µm at V_{gs} = 5 V and V_{ds} = 3.5 V. The threshold voltage (V_{th}) is around -9 V, indicating a highly depleted-mode device due to unintentional n-type doping of the MoS_2 during growth and fabrication. This is common for both CVD and exfoliated MoS_2 devices, which in recent studies has been attributed intrinsically to sulfur vacancies in the MoS_2 and extrinsically to doping resulting from the interfacial O vacancies at the MoS_2 – HfO_x interface. As a result of the oxygen vacancies, the uncompensated

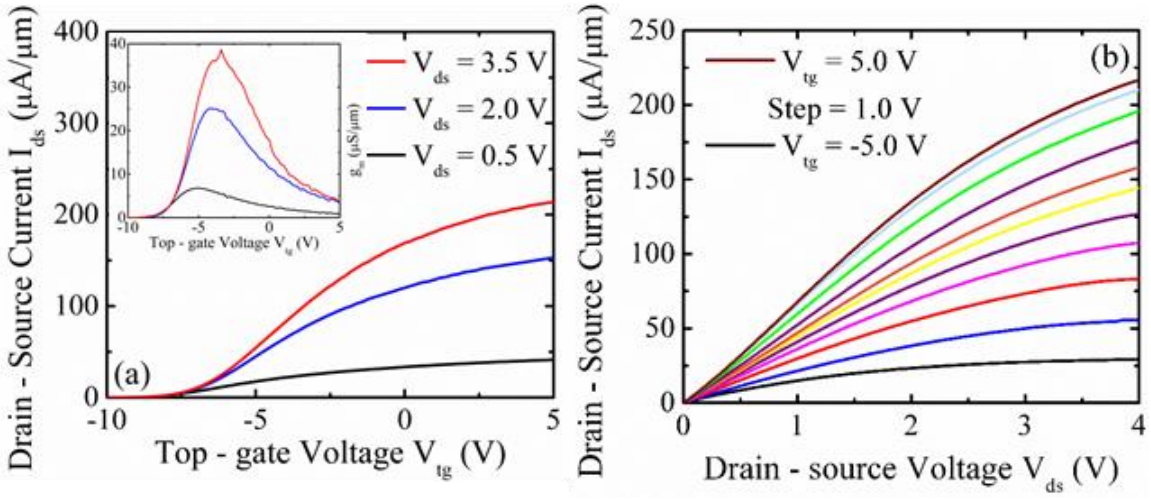

Figure 2.5: The back gate was grounded in all measurements. (a) I_{ds}-V_{gs} transfer curves of a CVD MoS_2 RF FET. The current density exceeds 200 μA/μm at V_{gs} = 5 V and V_{ds} = 3.5 V. The inset is the g_m-V_{gs} transconductance curves. The peak g_m is 38 μS/μm biased at V_{gs} = -4.5 V and V_{ds} = 3.5 V. (b) I_{ds}-V_{ds} output curves of a CVD MoS_2 RF FET. The V_{ds} is swept from 0 V to 4 V with different V_{tg}. The V_{tg} is swept from -5 V to 5 V in steps of 1 V. These curves are used to find the minimum drain conductance g_{ds} from which the voltage gain $A_v = g_m/g_{ds}$ is determined.

hafnium atoms at the MoS_2 surface lead to the creation of donor states near the conduction band of monolayer MoS_2, resulting in n-type charge transfer doping [32, 33]. The Hf:O ratio in our ALD HfO_x film was estimated to be ~1:1.56 from x-ray photoelectron spectroscopy (XPS), thereby confirming the oxygen deficiency. Furthermore, the doping of the MoS_2 channel upon ALD HfO_x encapsulation was confirmed by the red shift and peak broadening of the out-of-plane A_{1g} Raman mode of MoS_2. It can be surmised that this interfacial-oxygen-vacancy mediated doping of MoS_2 by the as-deposited ALD HfO_x layer is primarily responsible for the enhanced performance of our CVD MoS_2 FETs [32, 33, 34]. This n-doping would help reduce the contact resistance due to thinning of the Schottky barrier width along the Ag-MoS_2 contact regions. Moreover, the increased electron sheet density in the MoS_2 channel would result in improved screening of the substrate charged impurities and softening of the A_{1g} phonon modes of MoS_2, even before the application of external electrostatic biases. The inset of Figure 2.5(a) shows the g_m-V_{gs} transconductance curves for the CVD MoS_2 FET. The device achieves a maximum g_m of 38 μS/μm at V_{gs} = -4.5 V and V_{ds} = 3.5 V. Using the I_{ds}-V_{gs} transfer curves at a low-field V_{ds} of 0.01 V and a

TMD FET device model [35], we extract estimates for mobility and contact resistance to be μ_{FE} = 55 cm^2/Vs and R_c = 2.5 kΩ·μm.

2.5 TOP-GATED CVD MoS_2 FETS RF CHARACTERIZATION

The radio frequency performance of CVD MoS_2 can be evaluated from the transit frequency f_T. The frequency at which the current gain ($|h_{21}|$) is unity (0 dB) is the f_T of the device. In order to measure the transit frequency, an Agilent Microwave Network Analyzer (VNA-E8361C) was used for RF characterization in the range of 100 MHz to 10 GHz. To determine the intrinsic frequency performance of CVD MoS_2 FETs, standard OPEN and SHORT structures were used to de-embed parasitic capacitances and resistances. These structures were fabricated in close vicinity to the device-under-test (DUT) on the same substrate with identical layouts. The as-measured S-parameters were extracted from a monolayer CVD MoS_2 device with L_g = 250 nm and W = 20 μm. The short circuit current gain $|h_{21}|$ vs. frequency is shown in Figure 2.6(a). Operating at V_{gs} = -4.5 V and V_{ds} = 3.5 V corresponding to the maximum g_m point, the device extrinsic f_T is measured to be 2.8 GHz. After applying de-embedding parameters, the intrinsic f_T reaches 6.7 GHz [36]. The device shows good linearity in the log-scale with the expected -20 dB/dec slope. A higher f_T can be achieved by improving the g_m (by shortening the L_g), optimizing the layout to reduce parasitic capacitances, and reducing the contact resistance.

Another figure of merit for high-frequency transistors is the maximum frequency of oscillation, f_{max}. This is the frequency limit at which there is power gain given matched input and output impedances. The f_{max} of a FET depends on the drain conductance g_{ds}, which in turn depends on the saturation characteristics at the device operating point. The maximum available gain (MAG) was obtained from the measured S-parameters and is shown in Figure 2.6(b). Operating at the same DC bias point, we measure an extrinsic f_{max}

of 3.6 GHz. Using the same de-embedding procedure, the intrinsic maximum oscillation frequency is extracted to be f_{max} = 5.3 GHz. The f_{max} can be further improved by operating the device in deeper saturation to reduce $g_{ds,}$ by using a thicker gate metal to reduce gate resistance, and by reducing the access resistance at the contacts. In amplifier design, it is important to know the intrinsic voltage gain A_v. The intrinsic voltage gain can be extracted

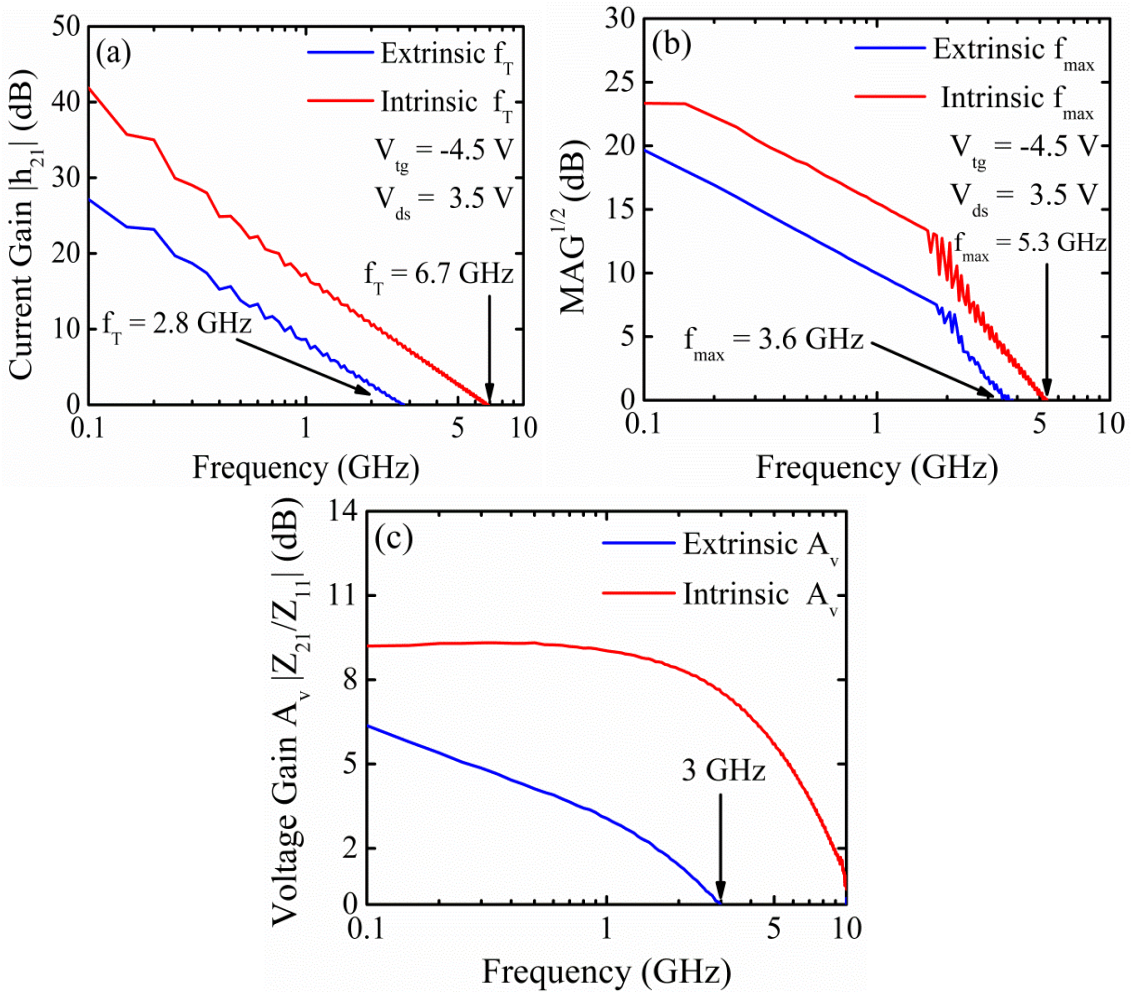

Figure 2.6: (a) Short circuit current gain $|h_{21}|$ vs. frequency showing an extrinsic f_T of 2.8 GHz and an intrinsic f_T of 6.7 GHz. The device shows good linearity with the expected -20 dB/dec slope. (b) Maximum frequency of oscillation f_{max} vs. frequency showing an extrinsic f_{max} of 3.6 GHz and an intrinsic f_{max} of 5.3 GHz. (c) Voltage gain A_v expressed in Z-parameters as Av = Z_{21}/Z_{11} vs. frequency. The Av is 6 dB at the minimum frequency 100 MHz and voltage gain is realized until 3 GHz.

from DC measurements as $A_v = g_m/g_{ds}$. The voltage gain can also be measured as a function of frequency by converting the S-parameters to impedance Z-parameters. Figure 2.6(c) shows the measured extrinsic and intrinsic voltage gain $A_v = Z_{21}/Z_{11}$. At 100 MHz, the extrinsic voltage gain is equal to 6 dB and voltage gain is realized until a frequency of 3 GHz.

2.5.1 VELOCITY SATURATION IN CVD MoS_2

The lateral electric field used for f_T measurement is in the high-field limit where carrier transport is determined by velocity saturation (v_{sat}). In this limit f_T scales inversely with channel length, hence, the frequency-length ($f_T \cdot L_g$) product is a useful metric for device performance benchmarking. The device RF measurements correspond to an $f_T \cdot L_g$ metric of ~1.68 GHz-μm, which is within the expected range for MoS_2. Furthermore, from the maximum f_T achieved, the carrier saturation velocity v_{sat} can be estimated using the high-field expression $v_{sat} = \frac{L_g}{\tau} = 2\pi f_T L_g$, where τ is the carrier transit time [37]. Using the device gate length of 250 nm, we extract $v_{sat} \approx 1.1\times10^6$ cm/s. This result is within a factor of 4 of theoretical estimates of monolayer MoS_2 saturation velocities based on DFT and Monte Carlo simulations [17, 38]. The effective velocity, v_{eff}, is shown in Figure 2.7 as a function of horizontal electric field (V_{ds}) for the RF MoS_2 device. It can be seen that the velocity does not change much in this high field regime of $V_{ds} > 3.5$ V. At these high electric fields the carrier velocity in the MoS_2 increases beyond the optical phonon energy. This increases the probability of carriers to emit an optical phonon, resulting in increased optical phonon scattering. The increased optical phonon scattering causes the carrier velocity to saturate with increased electric fields.

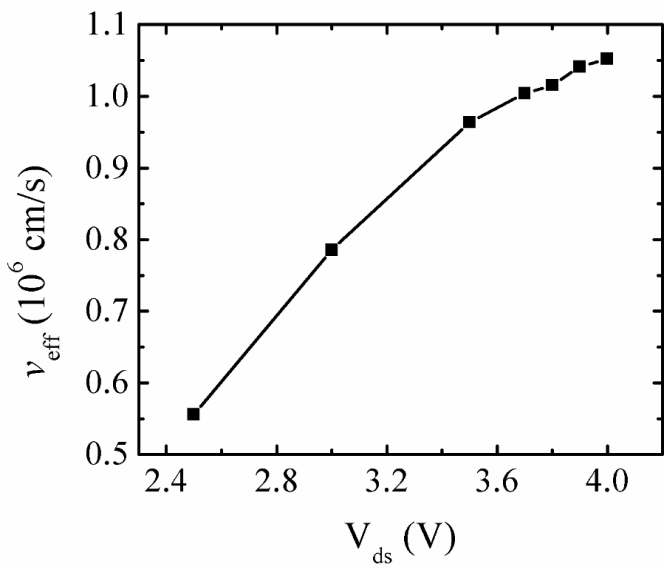

Figure 2.7: Effective carrier velocity v_{eff} as a function of drain voltage V_{ds}. The v_{eff} is extracted from the f_T measurement at different drain biases. The v_{eff} begins to saturate beyond a V_{ds} of 3.5 V, indicating the velocity saturation regime. This represents an upper limit to the f_T achievable. The gate length establishing the channel electrical field is 250 nm.

Further evidence of velocity saturation is evident in the scaling of f_T with gate length. In conventional non-velocity saturation regime devices $f_T = \frac{g_m}{2\pi(C_{gs})} = \frac{3}{4}\frac{\mu_n V_{OV}}{\pi L^2}$. Where C_{gs} is the channel capacitance and can be estimated as $C_{gs} = \frac{2}{3} W L_g C_{ox}$ in the saturation regime. Here it shows the f_T increase as the square of the decreasing gate length. The gm improves with decreasing L_g while improving the C_{gs} at the same time, hence the square dependence. This served to vastly improve achievable cutoff frequencies with early generation scaling. However in modern devices the magnitude of the operating electric fields bring saturation velocity into effect and the f_T scaling must be reexamined. Looking at the drain current in velocity saturation $I_{DS} \approx \frac{\mu_n C_{ox} W}{2} E_{sat}(V_{GS} - V_{th})$. We differentiate this expression with respect to the V_{gs} to get the transconductance $g_{m,sat} = \frac{\mu_n C_{ox} W}{2} E_{sat}$. Now the expression for f_T as a function of L_g is $f_T = \frac{g_{m,sat}}{2\pi(C_{gs})} = \frac{3}{4}\frac{\mu_n E_{sat}}{L_g}$. Here the f_T loses its square dependence and is now linearly improves with reducing gate lengths. The f_T and

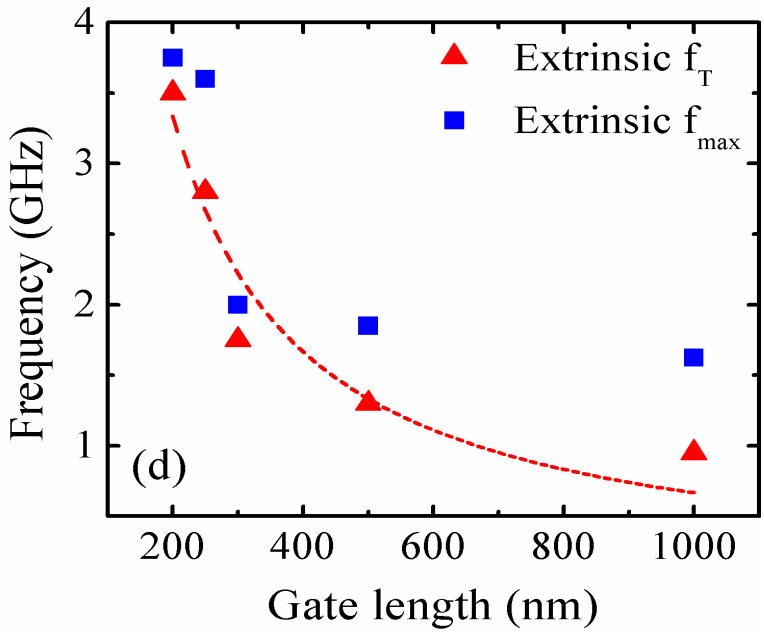

Figure 2.8: Extrinsic f_T and f_{max} as a function of gate length. The dashed line is a fit of the f_T-length data to a $\frac{1}{L}$ line. The close fit indicates the device operates in the velocity saturation regime where f_T scales inversely with length, as opposed to a square dependence in not velocity saturated operation. The f_{max} does not follow a particular trend.

f_{max} are measured at different gate lengths for MoS_2 RF FETs. Figure 2.8 shows the obtained extrinsic f_T values from gate lengths of 200 nm to 1 µm as the triangular data points. The dashed line represents a fit of the f_T data to a $\frac{1}{L}$ line. The close fit further confirms operation in the velocity saturation regime. The f_{max}-L_g relationship is also shown in Figure 2.8 as the square data points. The scaling of f_{max} does not follow the same $\frac{1}{L}$ trend as f_T. This is because individual device parameters such as gate resistance and output conductance affect the f_{max} for any particular gate length.

2.6 TOP-GATED CVD MoS_2 FET CIRCUIT DEMONSTRATION

High mobility, current saturation, GHz frequency performance (f_T and f_{max}), and high voltage gain motivated us to implement analog circuits using our monolayer CVD MoS_2 FETs. We designed and fabricated a common source (CS) amplifier and an active mixer using CVD monolayer MoS_2. In order to measure the MoS_2 DUT circuit operation, a test setup had to be established incorporating the probe station used to contact the fabricated devices. Figure 2.9 is a picture of the test equipment used during device and circuit measurement. Starting from the left of the image, the PNA (VNA) was used for 2-port high frequency performance device characterization. The oscilloscope is used to measure the circuit output waveforms and is equipped with the 1 MΩ input impedance.

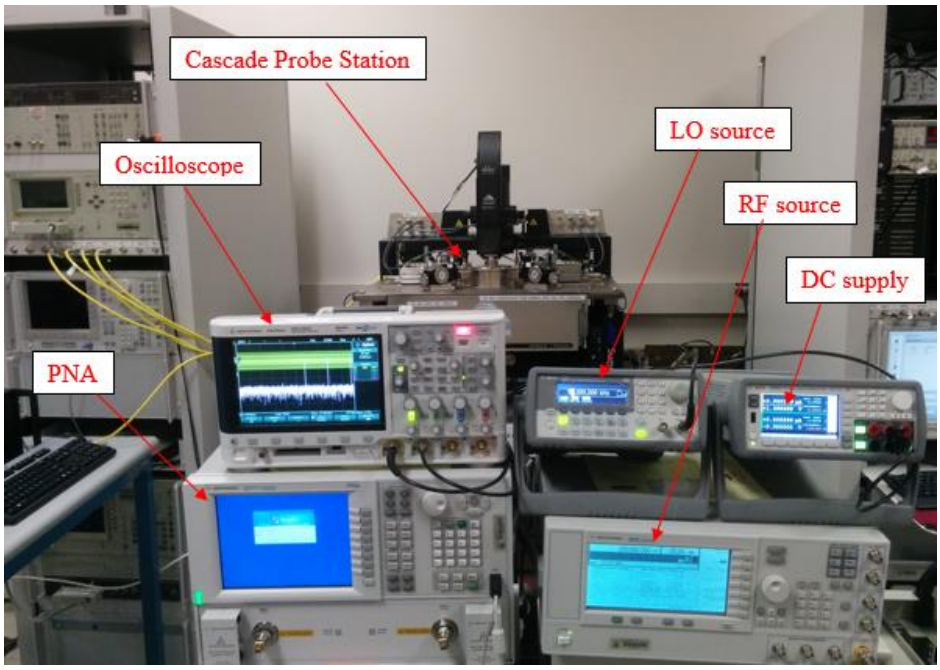

Figure 2.9: Test setup showing the various equipment used during circuit and device measurement. Starting from the left the PNA (VNA) was used for 2-port high frequency performance device characterization. The oscilloscope is used to measure the circuit output waveforms and is equipped with the 1 MΩ input impedance. The probe station houses the fabricated device. The LO and RF source are two function generators used as input signals. And finally the DC supply provides the device bias.

The probe station houses the fabricated device. The LO and RF source are two function generators used as input signals. And finally the DC supply provides the device bias. Not shown are the bias tees which were used to couple the RF and DC signals together. A major challenge is establishing the test setup is maintaining uniform connection types throughout the various equipment. For example, the oscilloscope and supplies all are connected with a triaxial BNC connector, whereas the device is probed with high frequency coaxial cables. Converting between these different types of connectors can provide frequency limitations, as seen in out experiments. As discussed in the future work section, a fully wire-bonded device with on-PCB discrete components serves as an ideal measurement setup where the intrinsic device performance can be achieved.

2.6.1 MoS_2 Common Source-Amplifier

A common-source (CS) amplifier is a basic building block for larger analog circuit amplifier blocks. The basic idea of a voltage amplifier using a MoS_2 FET is to use the transconductance of the device to convert variations in the input voltage to a small-

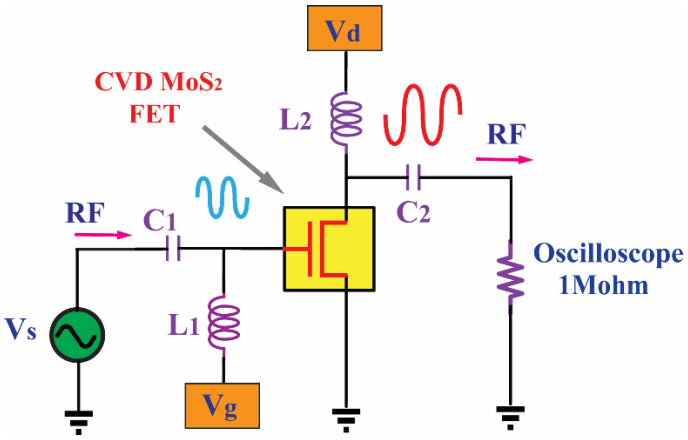

Figure 2.10: Circuit diagram of the measured CVD MoS_2 common source amplifier. The input RF signal V_s is applied to the gate while the output RF signal is measured across the oscilloscope input impedance of 1 MΩ. The DC signals required to bias the device are coupled with the small-signal RF signals using a bias-tee, which is represented by the $C_{1,2}$ and $L_{1,2}$ combination.

signal drain current, which can then be converted back to an output voltage with a resistor. The CS stage performs this operation by taking an input voltage into the FET gate (Vin) and outputting a voltage at the drain terminal (V_{out}), hence the source of the device is kept at the common mode. Figure 2.10 is a circuit diagram of the measured CVD MoS_2 CS amplifier. The input RF signal Vs is applied to the gate while the output RF signal is measured across the oscilloscope input impedance of 1 MΩ. The DC signals required to bias the device are coupled with the small-signal RF signals using a bias-tee, which is represented by the $C_{1,2}$ and $L_{1,2}$ combination.

The gain of a CS amplifier can be determined from the small-signal model of the FET. The open-circuit voltage gain (low-frequency) of CS stage is $-g_m(r_o||R_L)$, where g_m is the FET transconductance, r_o is the FET output resistance, and R_L is the load resistance. To find the intrinsic device voltage gain, the R_L has to be set large so the output resistance dominates the parallel combination. The MoS_2 FET is biased at the

same maximum transconductance point (V_{gs} = -4.5, V_{ds} = 3.5). Applying an input sine wave at 1.4 MHz we measure a voltage gain ($A_v = V_{out}/V_{in}$) of 14 dB (Figure 2.11). As mentioned in the previous section, the test setup with BNC to coaxial converters introduces a pole in the system, limiting the achievable frequency of operation. With perfect RF impedance tuners and noise matching circuits, the maximum achievable frequency of operation with at least unity gain is represented by the device f_{max}. With these measurement and circuit modifications introduced we expect operation of MoS_2 low noise amplifiers (LNAs) in the GHz range. The gain and frequency of the CS amplifier can be increased by optimizing the layout to reduce parasitic contact resistance and by employing a cascode circuit topology to mitigate parasitic capacitance effects.

2.6.2 MoS_2 FET Active Mixer

An active mixer takes advantage of the controlled non-linear nature of a device to produce various sum and difference harmonics of two input signals. They are commonly

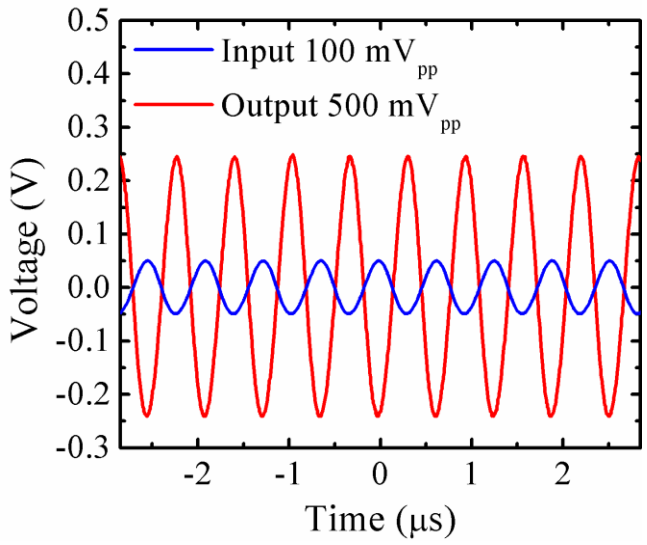

Figure 2.11: CS amplifier input and output measured waveforms. Applying an input sine signal at 1.4 MHz with a peak-to-peak voltage V_{pp} = 100 mV, we measure an output signal of V_{pp} = 500 mV. This corresponds to a voltage gain A_v = 5 (14 dB).

used in superheterodyne receivers and transmitters as downconverting or upconverting stages, demodulators, or modulators. Figure 2.12 is a circuit diagram of the measured MoS_2 active mixer. The RF signal represents a high frequency signal which may be downconverted through the introduction of a local oscillator (LO) signal. The LO signal may be generated on the same die from a voltage-controlled-oscillator (VCO) and can be tuned to a desired frequency. The two signals are power combined and fed to the gate of the MoS_2 FET. At the output, the sum and difference harmonics of the input signals are generated at the gain or loss provided by the active conversion of the FET. Below is a simple derivation of the output signal as a function of the input RF and LO signals mixed by the FET. The CVD MoS_2 FET gate input signal is given by:

$$v_g = A_{rf}\cos(\omega_{rf}\, t) + A_{lo}\cos(\omega_{lo}\, t) \qquad (4)$$

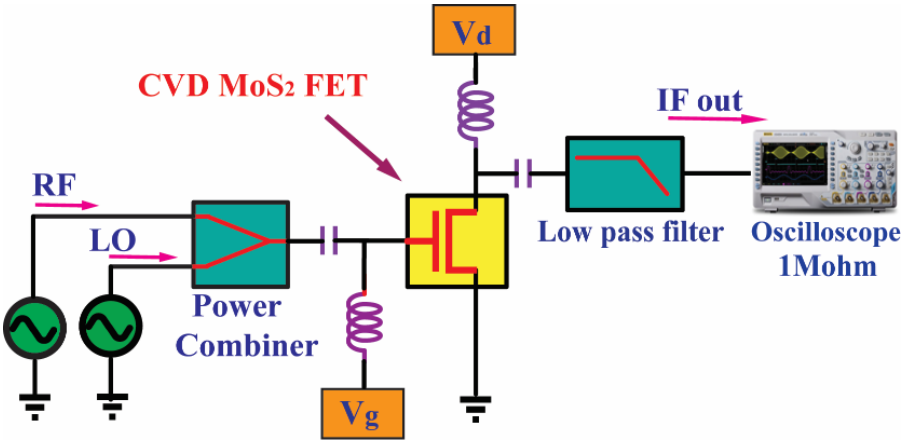

Figure 2.12: Circuit diagram of the measured CVD MoS_2 active mixer. The input RF signal is combined with a LO signal using a power combiner, and sent to the gate of the FET. The DC signals required to bias the device are coupled with the small-signal RF signals using a bias-tee.

where $A_{rf}$and ω_{rf} correspond to the amplitude and frequency of the RF input signal. A_{lo} and ω_{lo} correspond to the amplitude and frequency of the LO input signal. We have neglected the gate bias V_g to simplify the small signal analysis. The FET drain current is given by:

$$i_d = a_1 v_g + a_2 {v_g}^2 + higher\ order\ terms \qquad (5)$$

Substituting Equation 4 in Equation 5 and expanding:

$$i_d = a_1(A_{rf}\, cos(\omega_{rf}\, t) + A_{lo}\, cos(\omega_{lo}\, t)) + a_2(A_{rf}\, cos(\omega_{rf}\, t) + A_{lo}\, cos(\omega_{lo}\, t))^2 + higher\ order\ terms \qquad (6)$$

Expanding Equation 6:

$$\begin{aligned} i_d = {} & a_1 A_{rf} \cos(\omega_{rf}\, t) + a_1 A_{lo} \cos(\omega_{lo}\, t)) + a_2 \frac{{A_{rf}}^2}{2}(1 + \cos(2\omega_{rf}\, t)) \\ & + a_2 \frac{{A_{lo}}^2}{2}(1 + \cos(2\omega_{lo}\, t)) \\ & + A_{rf} A_{lo} a_2\, (\cos((\omega_{rf} - \omega_{lo})t) + A_{rf} A_{lo} a_2 (\cos(\omega_{rf} + \omega_{lo})t) \\ & + higher\ order\ terms \end{aligned} \qquad (7)$$

The drain current output of the mixer contains various intermodulation products (RF-LO, RF+LO, RF, LO, 2RF, 2LO). In Equation 7 the down converted signal is highlighted red and the up converted signal is green. Taking the down conversion case, the intermediate frequency (IF) is the desired mixer output defined as IF = RF – LO. A mixer is typically followed by a band pass filter which isolates the IF signal from the other unwanted harmonics. The conversion gain (CG) of the mixer is measured as the IF output power divided by the RF input power. From this derivation it can be seen that it is advantageous

that the FET is biased in deep saturation to maximize the non-linearity of the device. Also the intrinsic common-source gain the device provides to the mixing operation improves the CG, easing the requirements of successive gain stages.

In measuring the MoS_2 active mixer, we applied a 1.4 MHz RF signal with a 1.1 MHz (LO) signal. Our mixer measurement suffered the same frequency limitation as the CS amplifier due to the BNC to coaxial connector conversions. The drain output of the FET was connected to an oscilloscope where an FFT was taken. Figure 2.13(a) shows the frequency spectrum of the MoS_2 mixer output. It can be seen that the mixer is able to both upconvert and downconvert the inputs. Subtracting the gain provided by MoS_2 FET, and taking the IF and RF signal powers, we measure a conversion gain of about -15 dB (conversion loss of 15 dB). With improved layout and impedance tuners, higher conversion gain should be accessible. Figure 2.13(b) shows the mixer IF output power as a function of

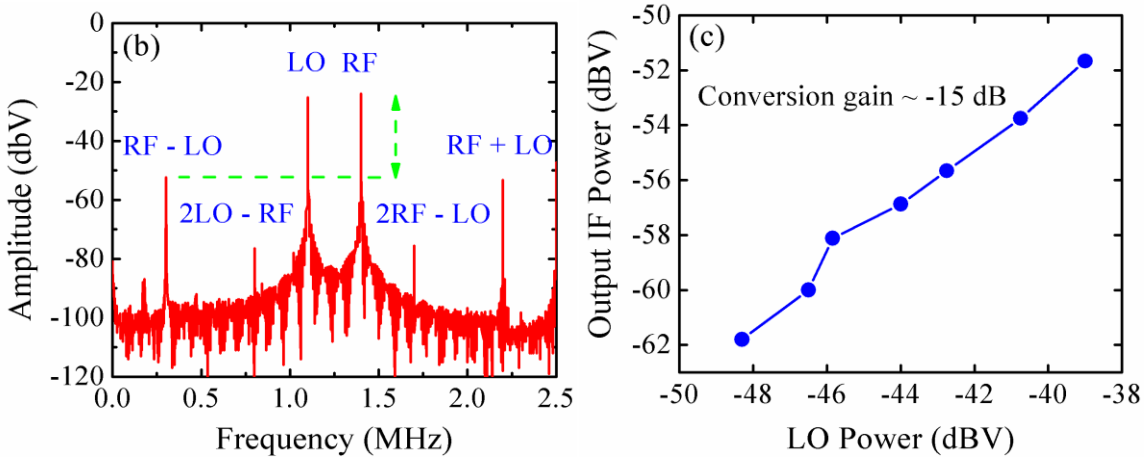

Figure 2.13: (a) Output FFT of a CVD MoS_2 mixer showing the input RF and LO signals and the expected intermediate frequency (IF = RF – LO) along with all the expected harmonics (2RF + LO, 2LO – RF…). The green arrow represents the IF conversion gain which after removing the signal gain is about -15 dB. (b) IF output power as a function of LO power. The MoS_2 mixer shows good linearity

LO power. The MoS_2 mixer shows good linearity, with a conversion gain between -12 dB and -16 dB. These results are promising for CVD MoS_2 low power superheterodyne mixers, modulators and demodulators, and radio receivers. Furthermore, this mixer is a single transistor mixer and further research is warranted to achieve differential amplifiers than can enable advanced mixer circuits such as the Gilbert cell topology that is widely used in contemporary CMOS circuits.

2.7 SUMMARY

In summary, the high frequency performance of top-gated CVD MoS_2 FETs was examined. First, the CVD-grown mm-scale MoS_2 was characterized by Raman and PL spectroscopy. The RF FETs were designed in the GSG structure for s-parameter extraction at high frequencies. In order to improve the current density of MoS_2 FETs, an oxygen-deficient HfO_x layer was employed as a gate dielectric. This served as a source of surface charge transfer doping, which induced a large negative V_{th} shift. The DC characterization of a 250 nm gate length device achieved a peak transconductance, g_m, of 38 µS/µm, leading to a contact resistance corrected mobility, µ, of 55 cm^2/Vs. The RF measurements of the CVD MoS_2 devices used standard OPEN and SHORT de-embedding structures to determine the intrinsic material performance. A CVD MoS_2 FETs with a L_g of 250 nm showed an extrinsic and, after de-embedding, intrinsic transit frequency, f_T, of 2.8 and 6.7 GHz, respectively. The extrinsic and intrinsic maximum oscillation frequencies, f_{max}, was measured to be 2.8 and 5.3 GHz, respectively. The channel length scaling of MoS2 FETs revealed a $\frac{1}{L}$ scaling trend of f_T. A plot of v_{sat} with increasing drain bias indicated the MoS_2 FETs operate in the velocity saturation regime, where a v_{sat} of 1.1×10^6 cm/s was extracted.

In addition, using the fabricated CVD MoS_2 RF FETs a CS amplifier and an active frequency mixer was measured. The CS amplifier showed a gain of 14 dB at an input frequency of 1.4 MHz. The MoS_2 mixer produced an intermediate frequency, IF, with a conversion gain of -15 dB. This chapter provides the initial findings of CVD MoS_2 RF device performance. The simple CS amplifier and mixer demonstrations provide a proof-of-concept for more complex high speed electronic circuits.

CHAPTER 3: Embedded Gate CVD MoS_2 RF FETs

3.1 INTRODUCTION

The embedded gate transistor has been well established in literature, particularly for the most prototypical 2D material, graphene [39, 40]. Graphene RF FETs using embedded gate transistors have achieved sub-THz cut-off frequencies [41]. However, the Dirac cone band structure of graphene results in a zero bandgap, which limits current saturation in graphene devices [42]. The embedded gate structure has been shown to significantly improve current saturation in graphene RF FETs, resulting in improved voltage and power gain. Embedded gate FETs using CVD MoS_2 for digital circuits were recently studied, which found increased scalability, with higher yield and uniformity versus their top-gated counterparts [43]. Figure 3.1(a) from ref. 43 shows the transfer curves for top-gated MoS_2 FETs compared to their embedded gate counterparts. There is an improvement in I_{ON}/I_{OFF} and a positive V_{th} is achieved in the embedded gate devices. In contrast to the previous chapter which showed large negative values for V_{th}, embedded gate CVD MoS_2 FETs have positive V_{ths}, showing enhancement mode operation. Enhancement mode operation is essential for complex multistage integrated circuits. Figure 3.1(b) shows the statistical spread of V_{th} of a batch of top-gated and embedded gate devices.

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Akinwande, and S. K. Banerjee supervised the work, and all authors reviewed and commented on the results and the manuscript. A. Sanne and S. Park are the corresponding authors for this publication.

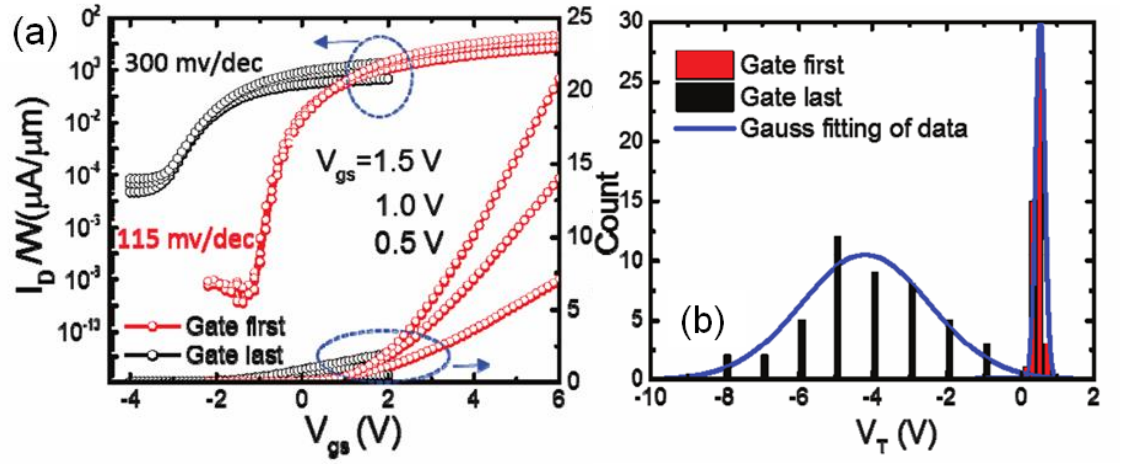

Figure 3.1: (a) Comparison of transfer characteristics of a gate-first and gate-last MoS_2 FET. The left scale is in a log scale while the right scale is linear. (b) Comparison of the V_{ths} of a batch of gate-first and gate-last MoS_2 devices. The data is fit to a Gaussian distribution. This figure is adapted from [43].

The common theme allowing improved performance among all 2D materials using embedded gates is a resist-free channel-dielectric interface with a reduced number of fabrication process steps after the transfer of the active material. Motivated by advantages described above, in this chapter, we employ the embedded gate structure to advance the RF characteristics of CVD MoS_2.

3.2 EMBEDDED GATE CVD MoS_2 RF FETS FABRICATION

The fabrication process for the embedded gate transistor begins with patterning two embedded gates on a substrate of choice. This is a main difference from the previously described top-gated flow. In the embedded case we refer to it as a gate-first process as compared with the gate-last process of the top-gated transistor. Figure 3.2 provides a graphical comparison of the two differing fabrication flows. Patterning the metal gates first

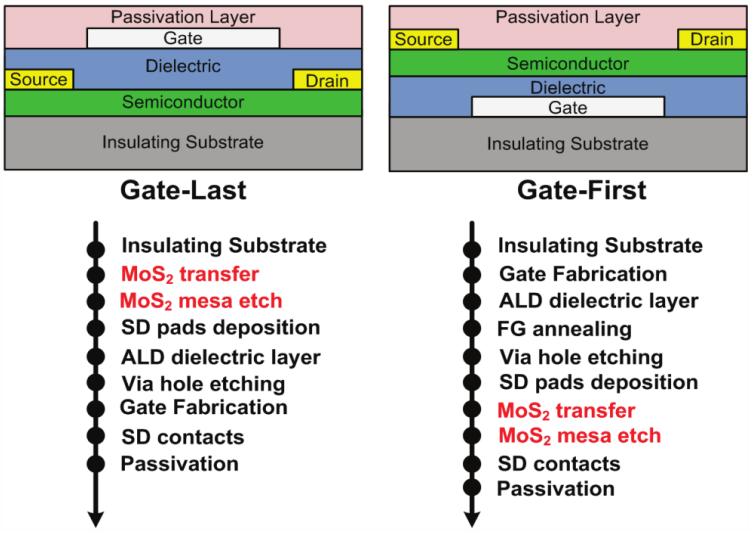

Figure 3.2: Comparison of the gate-first and gate-last fabrication process flows, where the former is an embedded gate transistor and the latter is a top-gated transistor. Note that in the gate-last case, the MoS_2 need not be transferred if it can be grown directly on the insulating substrate. This figure is adapted from [43].

has an impact on other fabrication steps within the flow. One example is that the CVD MoS_2 material must now be transferred upon the target metal gate, as opposed to the direct growth for top-gated transistors. The reason for this is the metal gate patterns cannot sustain the high growth temperatures required for the growth. Additional fabrication challenges are introduced such as considering the vertical height of the gate-first metal. The taller the metal gate, or finger, the longer the MoS_2 material must "drape" over the gate. This results in a longer gate length. One other point to be made relates to the ALD dielectric growth. In the gate-last case the ALD dielectric is grown directly onto the CVD MoS_2 material. This dictates that the oxide interfacing with the MoS_2 channel is formed from the initial cycles of the ALD. As discussed in the previous section, this results in a large number of oxygen vacancies (in the case of oxide dielectrics) which cause unintentional doping and large V_{th} shifts. In the gate-first case, the interfacing oxide is formed from the last cycles

of the ALD. We can surmise that the last cycles of the ALD are more stable than the initial cycles, resulting in a more stoichiometric oxide interface for gate first devices.

In our study the RF MoS_2 transistor fabrication begins with patterning two embedded gate fingers on intrinsic Si/SiO_2 (> 20k Ω·cm). Electron beam lithography (EBL) and e-beam evaporation were used to define and deposit the embedded gate metal stack consisting of 2/23 nm Ti/Au. Horizontal gate lengths were verified to be between 100 and 500 nm. The shortest total L_g is 150 nm; the sum of the horizontal length (100 nm) and the two heights of the sidewalls (50 nm). Atomic layer deposition (ALD) at 200 °C was used to deposit 10 nm of Al_2O_3 as the gate dielectric. Large area CVD MoS_2 was then transferred by poly(methyl methacrylate)-assisted wet transfer. A via to connect the embedded gate fingers with the gate pad was etched with phosphoric acid. The active MoS_2

channel was etched using Cl_2/O_2 plasma. A final EBL step patterned source and drain (S/D) contacts consisting of 2/70 nm Cr/Au. Figure 3.3(a) is a schematic of the cross-sectional view of the embedded gate device structure. As shown, the source and drain contacts do not overlap the gate. The underlap region is there to prevent parasitic C_{gs} and C_{gd} capacitances, but is minimized to reduce source and drain series resistance. Figure 3.3(b) shows an optical image of a fabricated CVD MoS_2 device array. The inset (bottom-right) shows the zoomed-in image of the gate fingers.

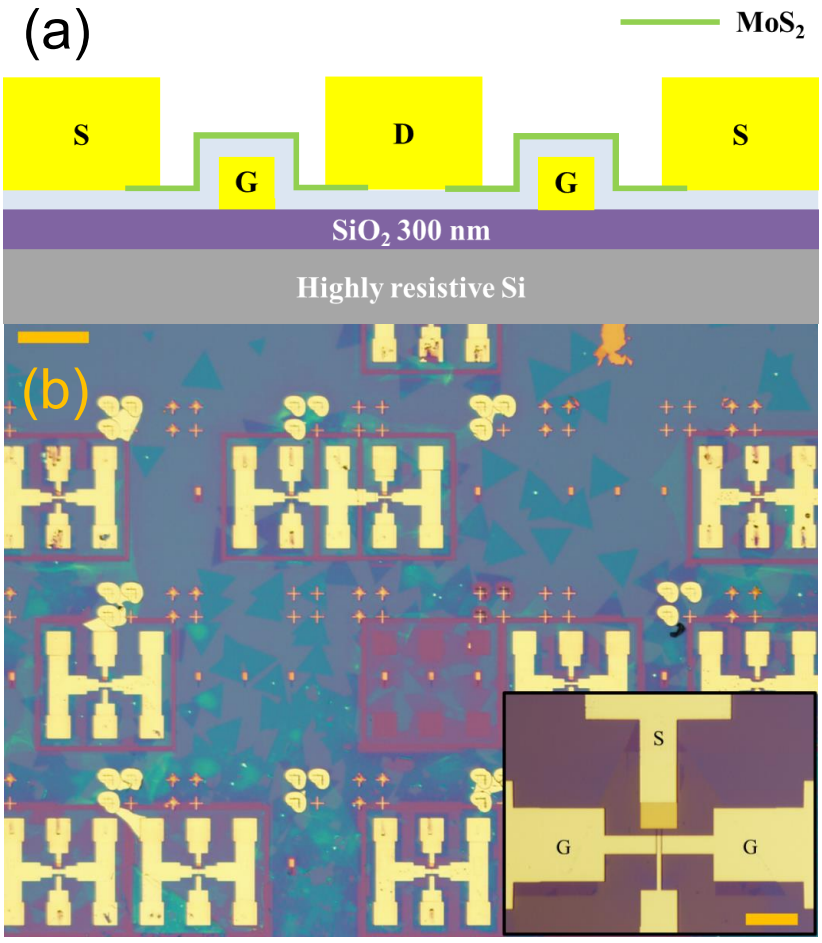

Figure 3.3: (a) A cross-sectional schematic of an embedded gate MoS_2 FET. (b) Optical image of a CVD MoS_2 device array with close-up gate finger layout (bottom-right inset). The scale bar for the array (top-left) is 200 µm and the scale bar for the inset (bottom-right) is 10 µm.

As with the material growth in the top-gated FETs, the MoS_2 was optically characterized in the embedded gate FETs. Figure 3.4 shows the Raman spectra of the as-grown and transferred MoS_2. The slight shift in the in-plane vibrational mode, E_{2g}, corresponds to a release of strain that exists in as-grown samples due to the mismatch of thermal coefficients between MoS_2 and the SiO_2 substrate.[14] The result of the same effect is also observed in the blue shift in the peak position of the photoluminescence spectra (Figure 3.4 inset).

3.3 EMBEDDED GATE CVD MoS_2 DC CHARACTERIZATION

Figure 3.5(a) shows the I_{ds}-V_{gs} transfer characteristics of an embedded gate MoS_2 FET with a physical gate length, L_g = 150 nm. The embedded gate structure preserves a clean MoS_2-dielectric interface with less fixed-charge and organic impurities. As a result, the threshold voltage, V_{th}, is positive and close to 0 V, as opposed to many top-gated structures, which suffer from uncompensated charge at the surface.[5] As shown in Figure

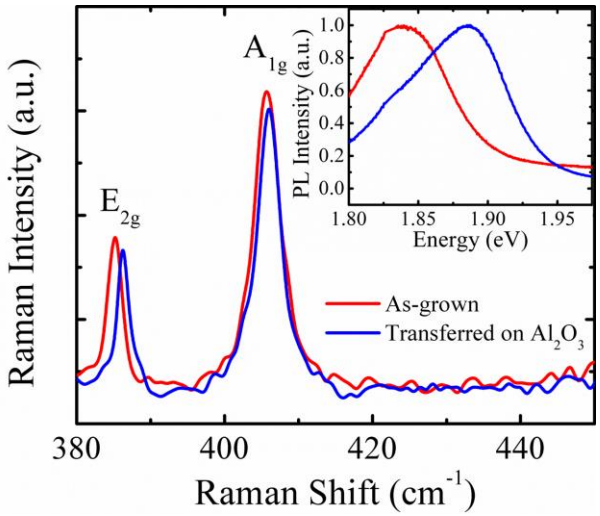

Figure 3.4: (a) Raman and photoluminescence (inset) spectra before and after transfer confirming the preserved CVD MoS_2 quality. The slight shift in the in-plane vibrational mode, E_{2g}, and the blue shift in the photoluminescence peak correspond to a release of thermal mismatch induced strain.

3.5(b), we measure a transconductance, g_m, of 70 μS/μm at a V_{ds} = 2.5 V. This is among the highest reported g_m for MoS_2 FETs on exfoliated or CVD grown films, at equivalent electric fields. The maximum field-effect mobility, μ_{FE}, is 21.2 cm^2/Vs, and after contact resistance correction is 81.6 cm^2/Vs. In addition to the improved MoS_2-dielectric interface, the embedded gate structure provides improved gate control over the channel. After transfer, the MoS_2 wraps conformed to the rectangular gate fingers. The electrostatic control is improved over top-gated devices because the electric field flux reaching the MoS_2 channel is increased at an equivalent gate voltage. As an enhancement mode device, we can sufficiently deplete the channel to achieve an I_{ON}/I_{OFF} ratio of 10^8.

Figure 3.5(c) shows the I_{ds}-V_{ds} output characteristics for the same device. The device achieves current densities of 120 μA/μm at V_{ds} = 3.5 V. There is clear current saturation beyond V_{ds} of 3 V, resulting in a drain conductance, g_{ds}, within 5 μS/μm in the current saturation region (3 V to 3.5 V of V_{ds}). The sub-linear curves at low V_{ds} indicate a significant Schottky barrier. We attribute this to undoped contacts and access regions. Our previous top-gated CVD MoS_2 RF FETs employed sub-stoichiometric $HfO_{1.56}$ which extrinsically doped the MoS_2 contacts and access regions. This n-doping helped reduce the contact/access resistance due to thinning of the Schottky barrier width. The difference in surface charge transfer doping between oxygen-deficient HfO_{2-x} and stoichiometric Al_2O_{3+x} has been observed and well quantified in literature. The $Al_2O_{3.1}$ used in this study

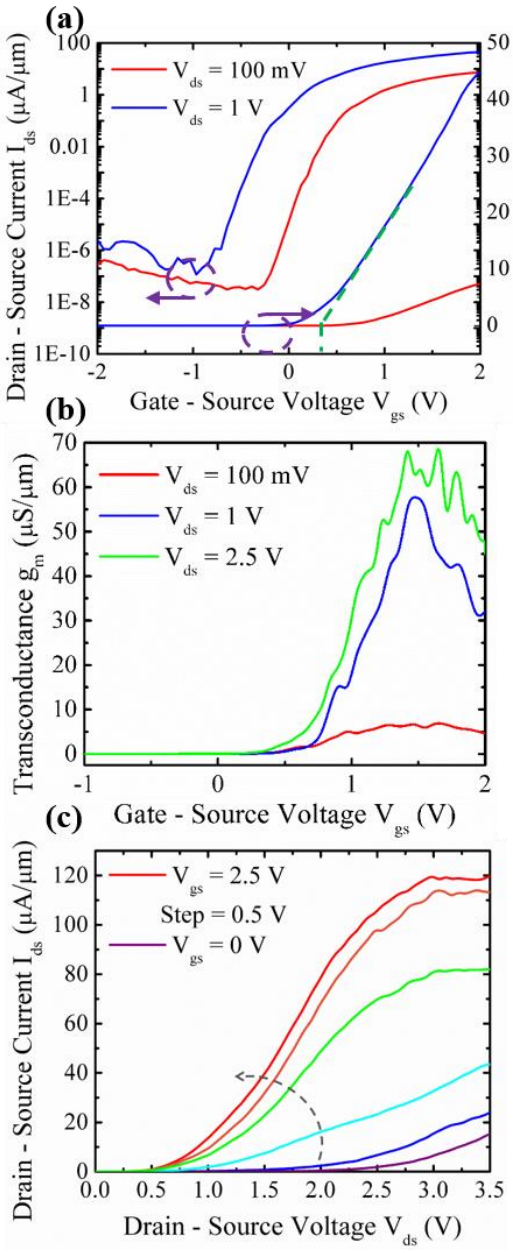

Figure 3.5: (a) Transfer curves, I_{ds}-V_{gs}, for a 150 nm gate length CVD MoS_2 device. The device shows enhancement mode operation with an I_{ON}/I_{OFF} ratio of 10^8 at 100 mV of drain bias. (b) Transconductance curves, g_m-V_{gs}, for the same device. The device has a peak g_m of 70 μS/μm at a V_{ds} of 2.5 V. (c) Output curves, I_{ds}-V_{ds}, for the same device. The device has a current density of 120 μA/μm at a V_{ds} of 3.5 V. The device shows current saturation beyond a V_{ds} of 3 V.

is oxygen-rich and closer to stoichiometric composition, providing minimal extrinsic

doping. As a result, the extracted contact resistance for the devices in this study is R_c = 3.5 kΩ·μm, which is larger than that our sub-stoichiometric $HfO_{1.56}$ devices. However, using a higher bandgap dielectric, alumina, and a carefully deposited uniform gate finger surface allows the scaling of dielectric thickness down to 10 nm. In these devices the top MoS_2 is exposed to ambient, allowing further dielectric/passivation layers or sensor measurements. The choice of top dielectric can provide the needed charge transfer to further improve the DC and RF characteristics.

3.4 EMBEDDED GATE CVD MoS_2 RF FETS RF PERFORMANCE

Microwave performance was characterized from 0.1-15 GHz using an Agilent two-port vector network analyzer (VNA-E8361C). To accurately subtract the effects of the parasitic capacitances and resistances in the ground-signal-ground (GSG) layout, we employed the standard de-embedding method using OPEN and SHORT measurements on the same device. Figure 3.6(a) shows the short circuit current gain $|h_{21}|$ versus frequency. Operating at V_{ds} = 3.5 V with L_g = 150 nm, we achieve an extrinsic f_T of 3.3 GHz and, after de-embedding, an intrinsic f_T of 20 GHz [44]. The lateral electric field used for the f_T measurement is in the high-field limit where carrier transport is determined by $v_{sat} = 2\pi \cdot f_{T,int} \cdot L_g$, and in our device is 1.88×10^6 cm/s. This is the highest extracted room temperature v_{sat} for any MoS_2 RF FET, either exfoliated or CVD. A higher f_T can be achieved by improving the g_m (by shortening the L_g), optimizing the layout to reduce parasitic capacitances, and reducing the contact resistance.

Figure 3.6(b) shows the maximum available power gain, f_{max}, versus frequency. Operating at the same DC bias, we measure an extrinsic f_{max} of 9.8 GHz and an intrinsic f_{max} of 11.4 GHz. This is the highest extrinsic f_{max} for all MoS_2 and the highest intrinsic

value for CVD MoS_2. We attribute the high f_{max} to good current saturation, leading to a small g_{ds} and a large output resistance, r_o. Figure 3.6(c) shows the scaling of f_T and f_{max} with gate length. The same principles of velocity saturation discussed in chapter 2 in the context of top-gated RF FETs applies to the embedded gate RF FETs shown here. In the high-field limit, the f_T generally scales inversely with length while f_{max} does not follow any trend due to varying individual device gate resistance and output conductance. In RF circuit

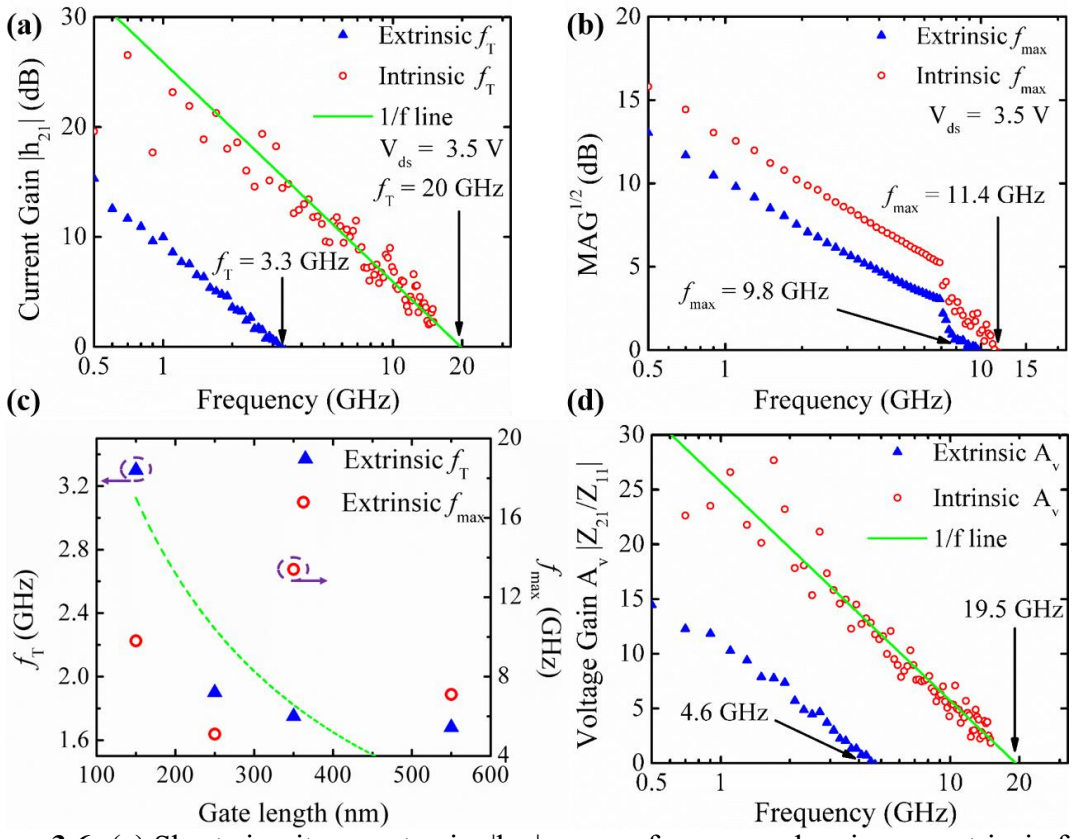

Figure 3.6: (a) Short circuit current gain, $|h_{21}|$, versus frequency showing an extrinsic f_T of 3.3 GHz and an intrinsic f_T of 20 GHz. The device shows good linearity with the expected −20 dB/dec slope. (b) Maximum available power gain, $MAG^{1/2}$, versus frequency showing an extrinsic f_{max} of 9.8 GHz and an intrinsic f_{max} of 11.4 GHz. We attribute the high f_{max} to current saturation-mediated low output conductance, g_{ds}. (c) Extrinsic f_T and f_{max} as a function of gate lengths from 150 - 550 nm. The dashed line is a fit of the f_T–L_g data to a 1/L line. (d) Voltage gain, A_v, expressed in Z-parameters as $A_v = Z_{21}/Z_{11}$ versus frequency. The extrinsic A_v gain is unity at 4.6 GHz. After de-embedding the unity gain frequency is 19.5 GHz.

design, it is important to know the intrinsic voltage gain A_v. The general expression for A_v is g_m/g_{ds}, but it can also be measured versus frequency with impedance Z-parameters. Figure 3.6(d) shows the extrinsic and intrinsic unity voltage gain cutoff frequency as 4.6 and 19.5 GHz, respectively. The outstanding RF device performance achieved here can be attributed to (i) a resist-free MoS_2-dielectric interface, (ii) a reduced number of fabrication process steps after transfer, compared with a top gate flow, and (iii) current saturation leading to a large r_o.

The intrinsic f_T is corroborated with the Gummel approach. Gummel's method provides an alternative method to measure the f_T using lower frequency values where the measured data may be more accurate. Derived from the common-emitter current gain Gummel's method states $h_{21}(f) = \frac{h_{21}(f=0)}{1+jh_{21}(f)\frac{f}{f_T}}$. Taking the imaginary portion of the inverse of this functions yields $Im\left[\frac{1}{h_{21}(f)}\right] = \frac{f}{f_T}$. From this we can observe that the slope of this function is the inverse of the fT. Figure 3.7(a) plots this function for the same intrinsic

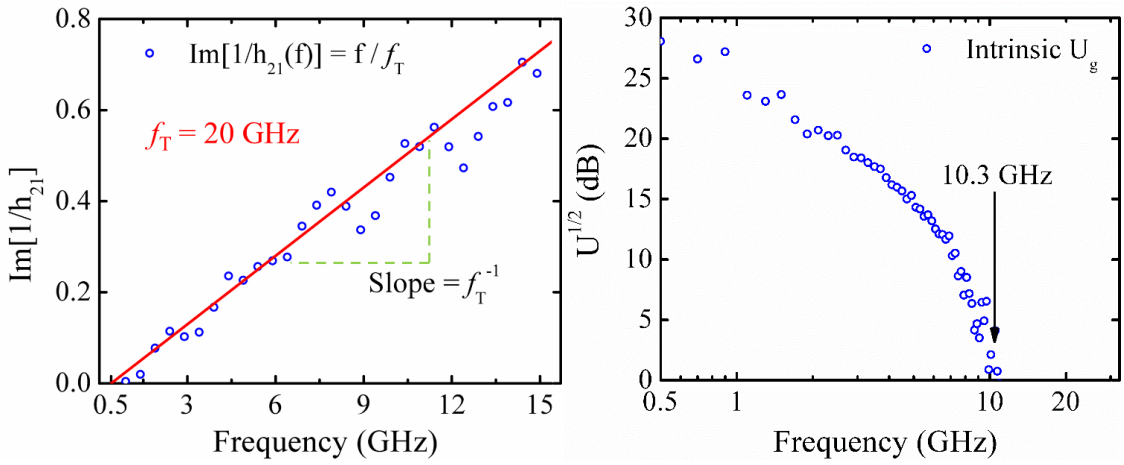

Figure 3.7: (a) Gummel's method of extracting f_T from the inverse slope of the $Im\left[\frac{1}{h_{21}(f)}\right]$. The inverse slope yields a f_T of 20 GHz which agrees with the current gain measurement. (b) Mason's unilateral gain plotted versus frequency. This method yields a f_{max} of 10.3 GHz which is close to the MAG/MSG measured f_{max}.

embedded gate FET data in Figure 3.6(a). The slope yields a f_T of 20 GHz, showing good agreement with the unity current gain value. We can also verify the f_{max} obtained from the MAG/MSG in Figure 3.6(b). Mason's unilateral gain (MUG, U) is the power gain of a 2-port network assuming no output-to-input feedback, or $S_{12} = 0$, and input and output to source and load conjugate matching, respectively. Figure 3.4(b) shows the MUG for the same embedded gate FET data in Figure 3.6(b). The frequency where the gain goes to unity is the f_{max} of the device, and from this method is 10.3 GHz, closely agreeing with the value obtained from the MAG/MSG.

Table 3.1 provides a summary of the currently reported MoS_2 RF data for both exfoliated and CVD devices. The embedded gate work in this section represents the highest

MoS_2 RF Literature Comparison							
Device	Configuration (active/substrate/ structure)	f_T ext/int (GHz)	f_{max} ext/ int (GHz)	A_V cutoff frequency ext/ int (GHz)	L_g (nm)	V_d (V)	v_{sat} ($\times 10^6$ cm/s)
[44]	CVD 1L/Si/ embedded gate	3.3/20	9.8/11.4	4.6/19.5	150	3.5	1.88
[15]	Exf 3L/Si/ top gate	1.9/14	-/14	-/29	40	2.5	0.35
[46]	Exf 3L/Si/ top gate with "edge contacts"	6/25	-/16	-/45	70	2.5	1.1
[16]	Exf 2-7nm/Si/ transferred gate	-/42	-/50	-/-	68	5	1.79
[18]	CVD 1L/Si/ top gate	2.8/6.7	3.6/5.3	3/11	300	3.5	1.26
[45]	CVD 1L/Flex/ top gate	2.7/5.6	2.1/3.3	-/-	500	2	1.76

Table 3.1: Comparison of RF MoS_2 FETs performance in literature. The saturation velocity, v_{sat}, calculated from the intrinsic f_T in embedded gate devices is the highest reported to date for both exfoliated and CVD MoS_2 RF systems.

saturation velocity, v_{sat}, taking into account both he measured f_T and the operating gate length. One exciting result from this table is the ability to retain a large saturation velocity even of flexible substrates. This shows promise for using MoS_2 in flexible wireless systems with a target operating frequency in the lower GHz regime.

3.4.1 EMBEDDED GATE CVD MoS_2 FETS DEVICE VARIABILITY

Variability is an important factor in obtaining high yield with device-to-device uniformity on a large-scale RF transistor integration. The sources of variability in the fabrication process presented here include intrinsic material non-uniformity, e-beam lithography, and local differences in the various device capacitances. Switching to a gas-based precursor system such as metalorganic chemical vapor deposition (MOCVD) can improve the material coverage and uniformity,[19] however, further work is needed to achieve the same device performance. A fully photolithographic process can help mitigate device-to-device feature size variations, which will also allow predictable device parasitics. To give some insight into the variability and scalability of our CVD MoS_2 RF devices, we studied the data from a single wafer device array where fabrication conditions were carefully kept uniform to accurately measure variability. Table 3.2 provides additional device data to give some insight into the reproducibility and scalability of CVD MoS_2 for RF devices. The devices were patterned on a single wafer and additional measures were taken to maintain uniformity among devices. We note that our fabrication process begins with 49 initial gate patterns on the bare SiO_2 substrate. After ALD and CVD MoS_2 film transfer, we identify which gate patterns are suitable for

Device Count	Maximum Current (uA/um)	g_m (uS/um)	u (cm^2/Vs)	I_{ON}/I_{OFF}	Extrinsic f_T
1	44.8	58.8	25.9	3.00E+08	3.25
2	22.4	43.1	21.36	3.00E+08	2.38
3	1.63	3.45	1.6	1.00E+03	0.19
4	0.67	1.32	0.49	7.00E+03	0.07
5	15.5	28.6	12.8	8.00E+06	1.58
6	3.62	8.68	3.2	4.00E+07	0.48
7	9.52	16.15	6.5	5.00E+08	0.89
8	0.07	0.13	0.05	1.00E+02	0.01
9	35.6	44.2	21.4	1.00E+08	2.44

Table 3.2: Device data of an array of fabricated CVD MoS_2 RF devices. The maximum current was measured at a V_d of 1 V and a V_{gs} of 2 V. The g_m is taken from a V_d of 1 V. The mobility is the raw field-effect mobility taken at a V_d of 100 mV. The I_{ON}/I_{OFF} ratio is for a V_d of 100 mV.

device completion, which came to a total of 15 potential devices. The count of device data seen below is the acquired functional data of the 15 attempted devices. Note that the non-functioning devices are not necessarily due to poor CVD MoS_2 sites, but were also caused by fabrication failures and electrical failures during biasing. An example of a fabrication failure is poor lift-off of the metal while an example of an electrical failure is gate breakdown during DC biasing. The maximum current was measured at a V_d of 1 V and a V_{gs} of 2 V. The g_m is taken from a V_d of 1 V. The mobility is the raw field-effect mobility taken at a V_d of 100 mV. The I_{ON}/I_{OFF} ratio is for a V_d of 100 mV.

3.5 EMBEDDED GATE CVD MoS_2 FETS CIRCUIT SIMULATIONS

Given the test measurement limitations experienced in the top-gated circuit demonstration, we chose to perform simulations using our measured DC and RF data to give some insight into MoS_2 circuit operation in more ideal cases. Two types of simulations were performed. One method is by using the measured s-parameters in a CAD simulation tool such as Advanced Design System (ADS) for high-frequency circuits. The other was

using a modified version of the MIT-MVS transistor Verilog-A model (using Cadence) for mixed-signal circuit simulation.

3.5.1 CVD MoS_2 Cascode Amplifier Circuit Simulation

Using the as-measured S-parameters, we designed a RF amplifier to demonstrate CVD MoS_2 as a viable material for a front-end low noise amplifier (LNA). We chose a cascode topology to minimize the Miller effect, provide input-output isolation, and improve the overall gain-bandwidth product. The amplifier schematic is shown in Figure 3.8. Figure 4(b) shows the amplifier gain (S_{21} in dB) and the input match (S_{11} in dB). We see a gain greater than 15 dB operating at 1.2 GHz, attributed to good current saturation. Figure 4(c) shows the input-output isolation greater than 20 dB at 1.2 GHz as afforded by

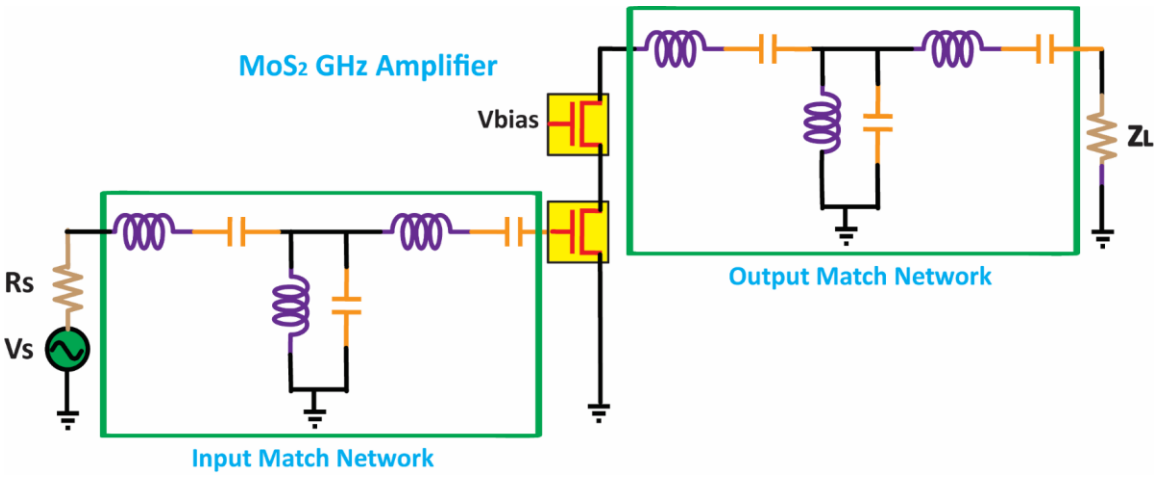

Figure 3.8: Circuit schematic for a MoS_2 GHz cascode amplifier. An input match network is used match to the 50 Ω source impedance. An output match network improves gain and bandwidth. The DC bias is not shown but can be provided by inductors connected to ground.

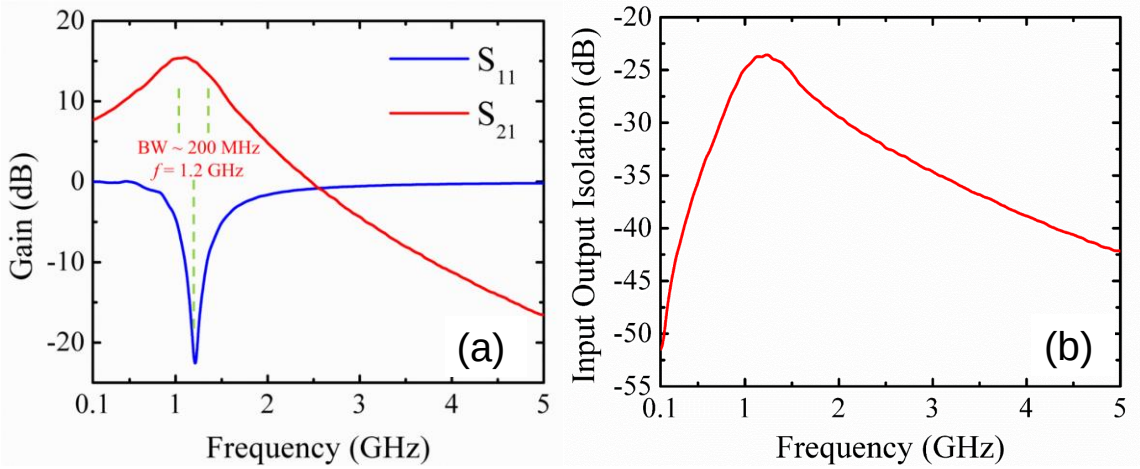

Figure 3.9: (a) The input match return loss, S_{11}, and the output gain, S_{21}, versus frequency. We see a gain greater than 15 dB at 1.2 GHz with a bandwidth of about 200 MHz and an input return loss better than 10 dB. (b) Input and output isolation versus frequency. The cascode topology allows better than 20 dB of isolation as it mitigates the Miller effect.

the cascode topology. The high gain of our front-end amplifier helps with setting the noise floor of the RF receiver. An input match network (IMN) is designed for matching the input impedance (Z_{in}) to the source impedance, R_s = 50 Ω. With the IMN we see input return loss greater than 10 dB. An output match network (OMN) is employed to improve the gain over the frequency bandwidth of 1.1 to 1.3 GHz. A standard Chebyshev Nth-order band pass filter topology can be modified for the design of the match networks.[20] We plan to further improve this design to take into account noise parameters for the practical design of MoS_2-based GHz LNAs.

3.5.2 CVD MoS_2 Mixed-Signal Circuit Simulation

In addition to high frequency simulations using measured s-parameters, a compact model for MoS_2 FETs was adapted from the MIT-MVS transistor Verilog-A model presented if ref 47. This model is advantageous for simulations as it requires only a few

physical measured values such as gate capacitance, C_{ox}, contact resistance, R_c, and mobility, u_{FE}. The model works by estimating the source and drain charge densities using self-consistent solutions for channel charge distribution. The model is referred as a virtual source as the current is evaluated at the source as $I_D = WQ_S v_{sat} F_{vsat}$ where F_{vsat} is a solution to the drift-diffusion transport equation which governs the transition from the linear to saturation region. Once the MoS_2 MVS model parameters are established and fit well to the experimental transfer and output curves, the FET cell can be used in conventional VLSI circuit design tools. The simulations shown here was done using the Cadence design suite. Figure 3.10 shows the circuit diagrams and simulated waveforms of three commonly used mixed-signal circuits – track and hold circuit (Figure 3.10(a)), full wave rectifier (Figure 3.10(b)), and an AM envelope detector (Figure 3.10(c)).

A track and hold (sample and hold) circuit is used in analog to digital converters as the front-end block which samples the input signal and holds it for subsequent data processing. The circuit consists of a single FET which serves as a pass-transistor switch to sample in the input V_s, and a capacitor, C_{load}, to hold the sampled value. The MoS_2 FET gate is controlled by a clock signal V_{clk}. As shown in the waveform, when V_{clk} is high the signal tracks the input and when V_{clk} goes low it holds the sampled value across the capacitor. There are several design considerations that go into the FET which is used as the sampling switch. One non-ideality is sampled charge leakage through the FET source or drain reverse-biased junctions. This causes the sampled value to degrade over time causing computational errors or limiting its window. A MoS_2 monolayer may have advantages over Si FETs in this aspect as the ultra-thin body precludes a requirement for a doped source and drain contacts. The MoS_2-based track and hold circuit shows a thermal noise limited SNR of 90.85 dB.

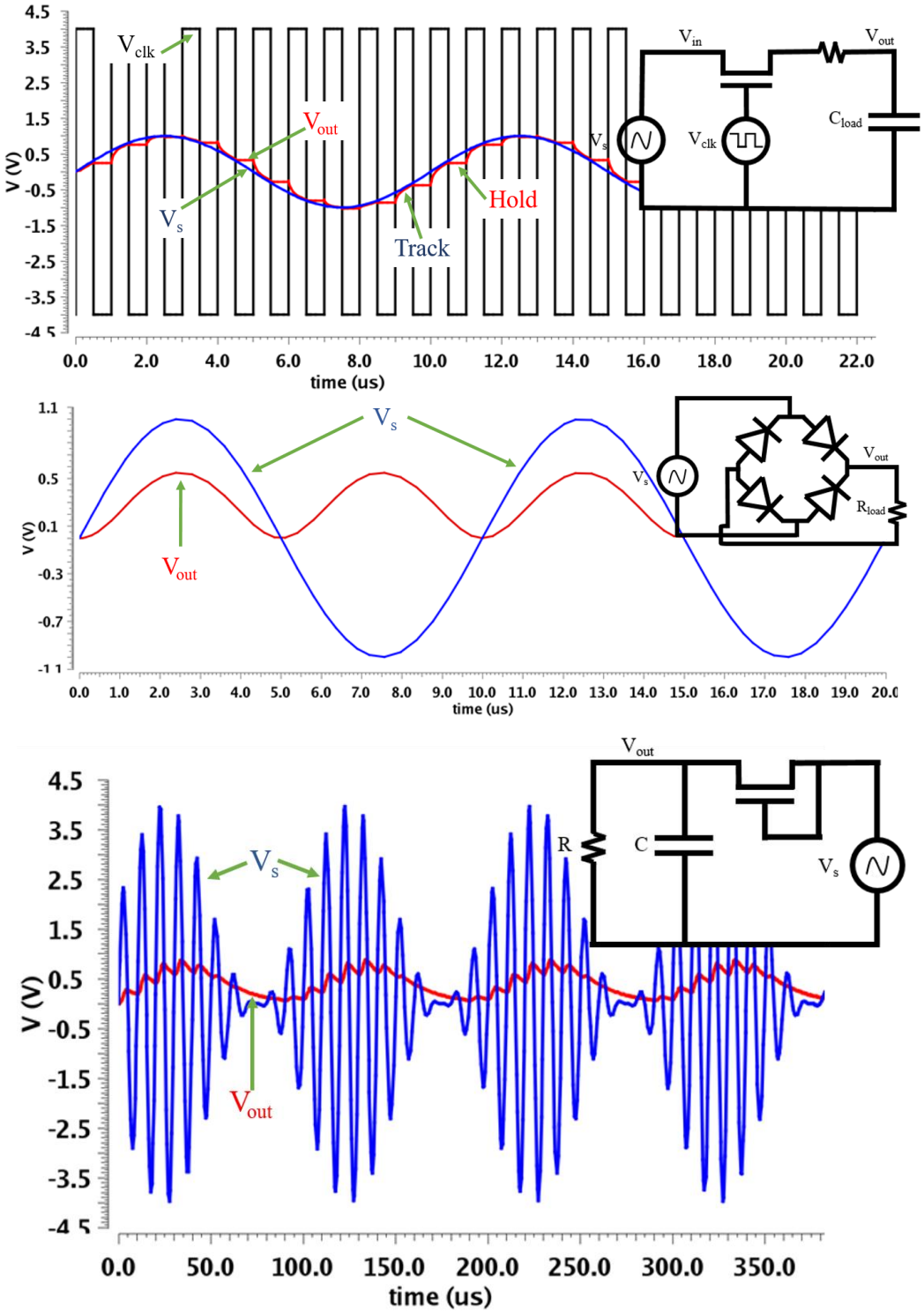

Figure 3.10: (a) Track and hold circuit and waveform modeled on a CVD MoS_2 RF FET. (b) Full wave rectifier circuit and waveform. (c) Envelope detector used for AM demodulation.

A full wave rectifier is used for AC to DC conversion. It can be coupled with a reservoir capacitor to smooth the ripple of the output DC signal. The circuit is composed of four diodes connected in a "bridge" configuration. During the positive half-cycle two of the diodes conduct in series while the other two are reverse-biased. The opposite occurs during the negative half-cycle.

An AM envelope detector is used in the demodulation of AM radio signals. The circuit in its simplest form is a diode-connected FET which charges a capacitor depending on the amplitude of the input signal. When in the input signal falls the resistors serves as a discharge path for the capacitor. The waveform shows a modulated input signal and an attenuated output signal which is the envelope of the input. The output is delayed compared to the input governed by the RC time constant of the circuit. The MoS_2 envelope detector here shows a peak attenuation of 13.8 dB.

3.6 SUMMARY

The large negative V_{th} shift in HfO_2 top-gated MoS_2 devices is undesirable for high speed complex multistage circuits. Embedded gate FETs use a gate-first process flow that ensures a stoichiometric oxide interface, devoid of organic contaminants, with the MoS_2. The DC characterization of Al_2O_3-gated CVD MoS_2 FETs show enhancement mode operation, with I_{ON}/I_{OFF} ratios of 10^8. Furthermore, the clean MoS_2-to-oxide interface improves the mobility and yields a maximum transconductance, g_m, of 70 μS/μm. High frequency characterization of a L_g = 150 nm embedded gate CVD MoS_2 FET achieved an extrinsic and intrinsic transit frequency, f_T, of 3.3 and 20 GHz, respectively. The maximum oscillation frequency, extrinsic and intrinsic f_{max}, was measured as 9.8 and 11.4 GHz, respectively. The de-embedding was done using the OPEN and SHORT method on the

same DUT for accurate parasitic removal. Gate length scaling of embedded gate MoS_2 FETs shows f_T to improve as $\frac{1}{L_g}$, consistent with the high-field velocity saturated limit. From the high field f_T measurement the v_{sat} is extracted as 1.88×10^6 cm/s.

Chapter 2 showed the circuit demonstration of a common-source amplifier and a mixer using a CVD MoS_2 FET. In order to utilize more complex circuit functions, the integration of multiple transistors is required. In order to better understanding the performance targets of MoS_2 in this context, a CVD MoS_2 cascode amplifier, consisting of two MoS_2 FETs in series, was simulated using the measured s-parameter data. The simulation was done using input and output matching networks without any parasitic non-idealities. The results showed MoS_2 cascode capable of gain in the GHz regime, where the low return loss and isolation properties are preserved. To briefly examine even more complex circuits, a sample and hold circuit, full wave rectifier, and an AM demodulator was simulated for CVD MoS_2. The simulations were done using a CAD design-compatible virtual source Verilog-A compact model with input measured device small-signal parameters. The initial results show promise for CVD MoS_2 use in analog and mixed-signal circuits.

CHAPTER 4: CVD MoS_2 Cascode

4.1 INTRODUCTION

In chapter 2, a common-source (CS) amplifier was demonstrated consisting of a single MoS_2 FET. In chapter 3 the simulation results of simple mixed-signal circuits based on CVD MoS_2 experimental data was presented. In order to determine MoS_2 as a capable material to employ in large area integrated-circuits, multi-transistor circuit demonstration is required. While multi-transistor integrated MoS_2 circuits have been demonstrated for digital circuit operation, there has been limited work on analog circuits. A natural circuit to attempt in succession to the previously measure CS amplifier is a cascode amplifier. In this chapter the design, fabrication, and measurement of a CVD MoS_2 cascode amplifier is outlined.

4.2 THE CASCODE AMPLIFIER

The cascode amplifier is a two stage circuit, the first being a CS amplifier, which is cascaded with a common-gate stage. Figure 4.1 shows a circuit schematic for a cascode amplifier. The input is applied to the gate of the bottom transistor M_1 (Q_1), often called the input transistor. M_1 generates a small-signal drain current governed by the input and the transconductance of the FET. The upper transistor M_2 (Q_2), also called the cascode transistor, forms a common-gate amplifier with its input as the drain of M_1 and its output as the overall cascode amplifier output, V_o. This can be viewed as M_2 simply routing the current from M_1 to the output, stipulating the current through the two FETs is the same. M_2 is DC-biased at its gate ($V_{gs,2}$) as to maintain itself in saturation. This bias is important as if it falls too low it forces the FET into the triode region, reducing the overall gain.

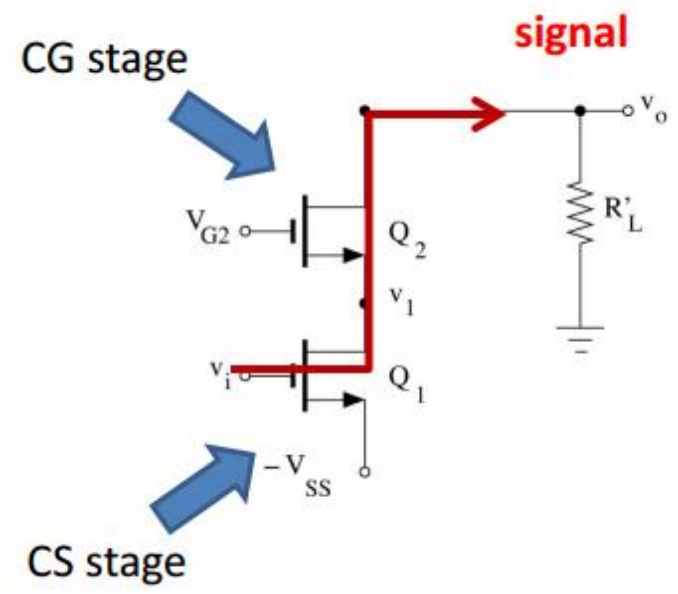

Figure 4.1: Circuit schematic of a cascode amplifier. The Q_1 (M_1) FET is the input CS stage and Q_2 (M_2) is the common-gate (CG) stage.

There are many advantages to the cascode configuration when employed as a high frequency amplifier. The cascode amplifier has a much larger output impedance as compared to the CS amplifier. The input impedance seen by M_2 is simple the output resistance of M_1, which is r_{o1}. The common-gate stage scales this impedance up from its source to drain by a factor of $g_{m2}r_{o2}$. This gives an output impedance of $R_{out} \approx g_m r_o^2$, assuming the output resistances of the two FETs are the same. Another way to look at the output impedance of the cascode is as a CS stage with a degenerated source resistance of r_o. A full small-signal output impedance calculation with independent output resistances yields $R_{out} = [1 + (g_m + g_{mb2})r_{o2}]r_{o1} + r_{o2}$, where g_{mb2} is the body bias transconductance generator for M_2, since its source and body terminals are at different voltages.

Another advantage of the cascode is its inherent shielding property. This proves useful at high frequency operation where the Miller effect is mitigated. The Miller effect

generalized occurs when there is an impedance across two nodes which has a voltage gain. In this scenario the equivalent input impedance seen across the nodes is multiplied by the gain. As it relates to analog circuits, a CS amplifier has its input at the gate of a FET and its output taken at its drain. From the small-signal model there is a C_{gd} capacitance across these nodes. The Miller effect creates an effective input "Miller" capacitance equal to the FET C_{gd} multiplied by the gain of CS stage, or $C_M = [1 + g_m r_o]C_{gd}$. The Miller effect is undesirable for high frequency operation as the poles of the system are associated with RC time constant at each node. The cascode configuration reduces the Miller capacitance of the CS amplifier by reducing the output impedance seen by M_1, which is now $\frac{1}{g_{m2}}$ (ignoring channel length modulation and the body bias of M_2) instead of r_o as in a standalone CS stage. As a result the overall gain is reduced, lowering the multiplicative effect on the feedback C_{gd}.

The benefits of the cascode amplifier can be summarized as following: higher input-output isolation, higher output impedance, and a higher gain-bandwidth product. In this chapter, the design, fabrication, and measurement of a CVD MoS_2 cascode is shown. Taking the learnings from the CS amplifier, a cascode transistor is designed in the GSG structure. However in moving from one to two transistors, additional challenges are encountered. The DC and RF characteristics of a fabricated cascode are measured.

4.3 CVD MoS_2 Cascode GSG Design

In order to characterize the high frequency performance of the cascode amplifier, the GSG configuration used for single FET measurements must be adapted. The same design principles for the single FET GSG structure apply for the cascode. Namely, the same pad landing rules must be maintained and the overall structure must be symmetric. A

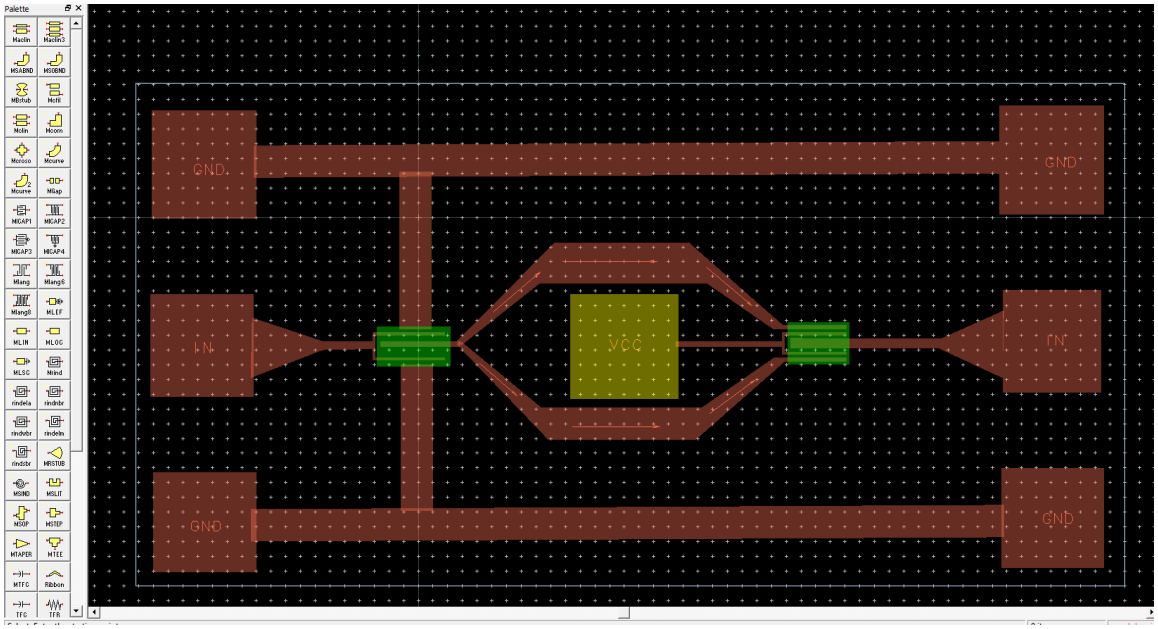

Figure 4.2: An ADS-generated schematic of a cascode in the GSG configuration. This design served as the basis for the initial MoS_2 cascode layout gds.

first pass design was generated using ADS as shown in Figure 4.2. From this image a gds file was created. Figure 4.3(a) is an optical image of a fabricated MoS_2 cascode based on the ADS-generated template. The V_i ($V_{gs,1}$) and V_o pads are the cascode input and outputs nodes, respectively. The V_1 node is the intermediate node contacting the two FETs together. The V_{G2} ($V_{gs,2}$) pad is the bias for the cascode transistor. This bias is not compatible with the GSG probes but it can be supplied with a separate individual DC probe, as it is not in the high frequency path. In this design the FETs are top-gated with the same process flow as that used in chapter 2. Figure 4.3(a) shows the two individual FETs far apart from each other in physical separation, about 100 μm. This presents a concern in that the two MoS_2 sheets used for the active FETs were grown far apart from each other. It is surmised that two MoS_2 sheets grown in a close vicinity to each other should show better matched electrical characteristics. If matching is poor and, for example, the V_{ths} of the two

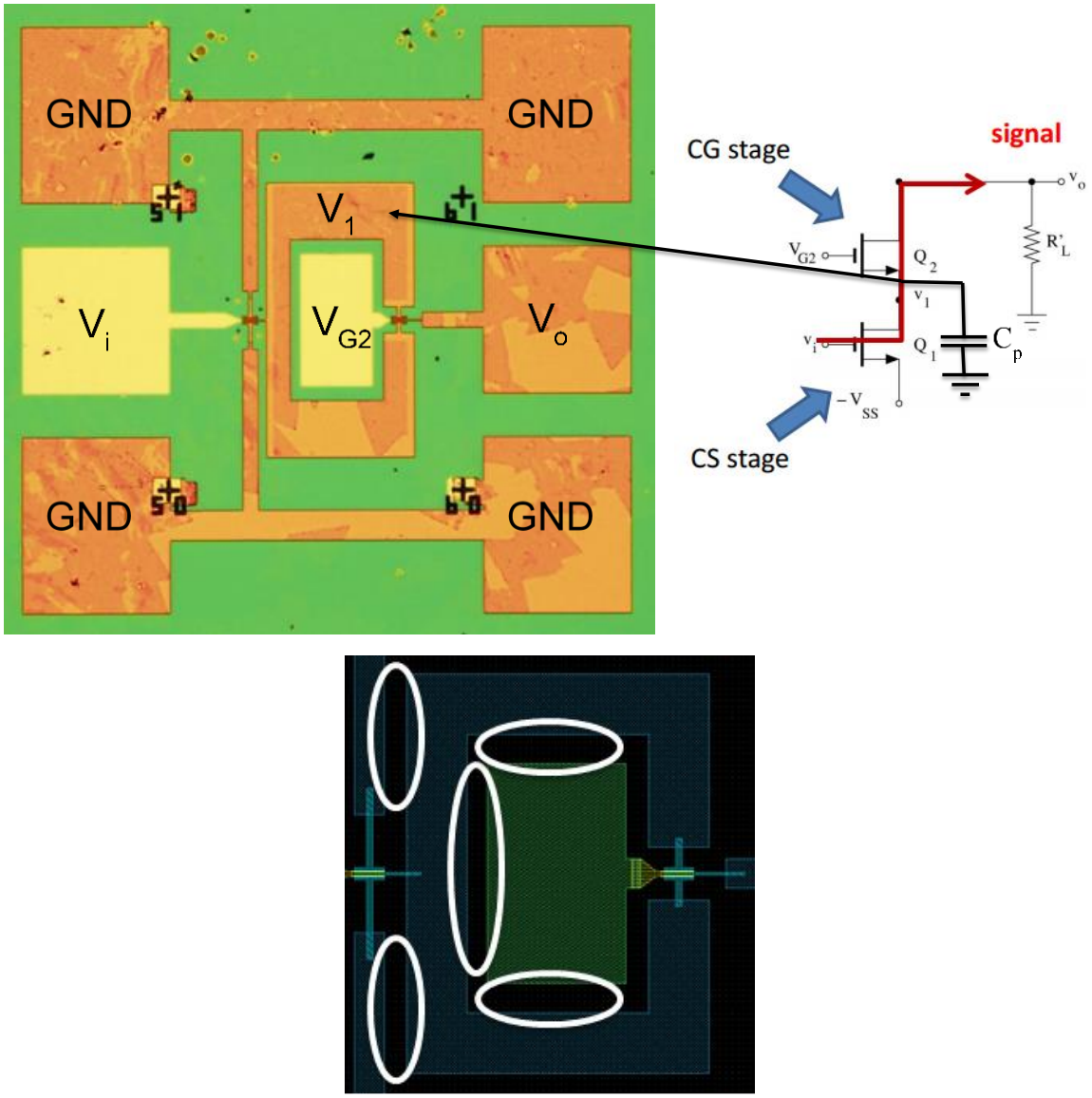

Figure 4.3: (a) Optical image of a CVD MoS_2 cascode circuit in the GSG configuration. The large V_1 node creates a parasitic capacitance with is modeled in the circuit diagram as a lumped capacitor, C_p. (b) Zoomed-in image of the V_1 node with circled areas indicating metal line-to-line parasitic capacitances.

FETs are far apart from each other, the biasing to put both FETs in saturation is challenging. Additionally if one FET shows a mobility much less than the other, the lower mobility will limit the overall performance.

An unforeseen design flaw in this cascode GSG structure is the intermediate node V_1. This metal trace was widened and composed of a thick metal stack to in an attempt to reduce the parasitic resistance between the two FETs. In making these choices the large capacitance at this node was ignored. Figure 4.3(a) models this V_1 node modeled as a lumped parasitic capacitor, C_p, in the cascode circuit diagram. As a result, this cascode amplifier achieved a very low f_T, about 100 MHz. The high frequency measurements yielded a high low frequency gain which rolled off non-linearly. There are two contributions to the parasitic capacitance created by the large V_1 node. First is the capacitance to substrate. This is a function of the areal coverage of the V_1 node. The highly resistive substrate with the thick substrate oxide helps to reduce this component. The second is the metal line-to-line sidewall capacitance. The circled portions of Figure 4.3(b) are large capacitors composed of metal trace sidewalls. Here the metal line separation is very short which is equivalently a thin oxide in a parallel plate capacitor. Figure 4.4 shows a simulation of the short-circuit current gain of a MoS_2 cascode. The simulation is performed using the previously measured s-parameters of a single MoS_2 FET. The three curves compare a single FET, a cascode, and a cascode with a parasitic capacitor, C_p, connected to the middle node. The cascode with a parasitic capacitor shows a sharp roll off. The pole created by the large intermediate node capacitance significantly reduces the bandwidth. The low frequency gain is larger for both cascode curves due to the improved output impedance. The middle node parasitic capacitance must be reduced to achieve higher cutoff frequencies for the cascode. The next section describes a layout redesign to reduce the parasitic capacitance

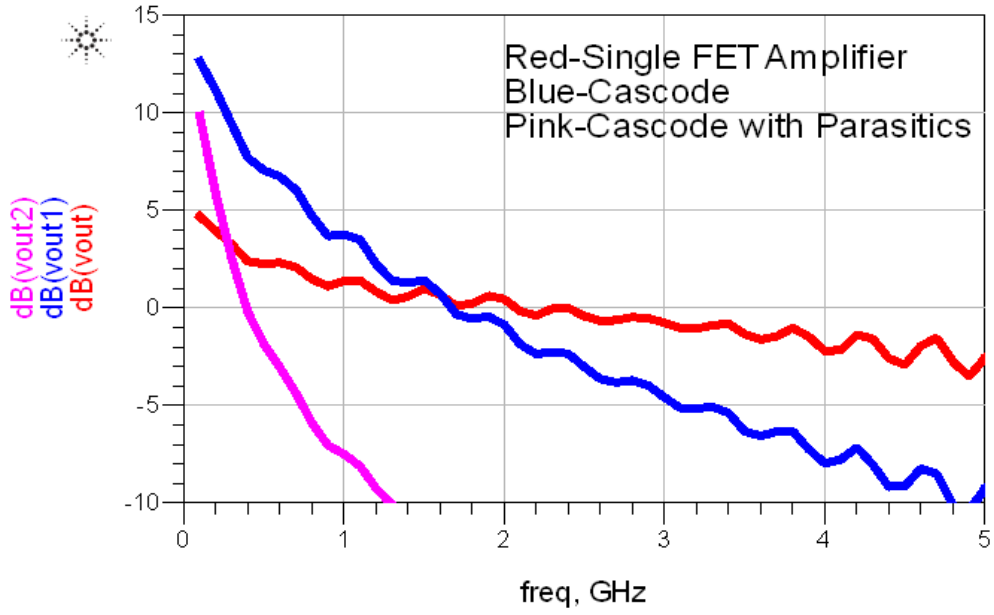

Figure 4.4: Short-circuit current gain simulations of a MoS_2 cascode high frequency behavior using the measured s-parameters of a single MoS_2 FET. The red, blue and pink curves are the frequency responses for a single FET, a cascode, and a cascode with a capacitor tied to the intermediate node.

4.3.1 CVD MoS_2 Cascode GSG Redesign

The goal of the cascode redesign is to reduce the metal trace and line-to-line capacitance area of the V_1 intermediate node, while maintaining GSG structure and overall symmetry. One observation is the V_{G2} bias pad in Figure 4.3 need not be placed in the center of the two FETs. Figure 4.5(a,b,c) shows the optical images of three cascode design variants which significantly reduce the V_1 intermediate node footprint. The Figure 4.5(a,b) redesign approaches split V_{G2} into two pads symmetrically about the horizontal axis of symmetry. The two pads are electrical connected together so only one probe is needed for bias. Here the V_1 metal trace is minimized both in area and line-to-line coverage. The only difference between the two design variants is that in Figure 4.5(b) the V_1 trace is connected

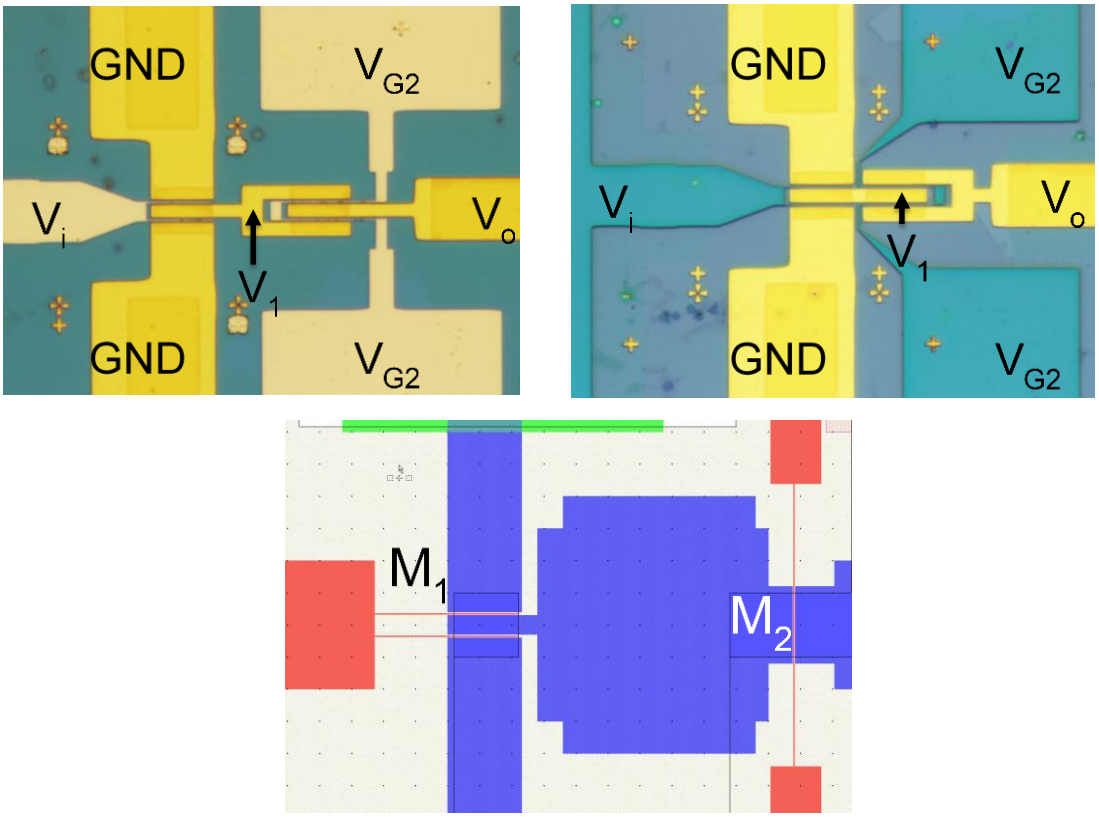

Figure 4.5: (a) Cascode redesign in the GSG structure with the V_{G2} pad split into symmetric pads. (b) Variation to the design in (a) which connects the V_1 trace to the center signal lines for both FETs, further reducing its footprint. (c) Cascode design variation where a single gate finger is used for M_2 with double the width.

to the center signal lines for both FETs, further reducing its footprint. The overall current density capability is the same for both layouts. Figure 4.5(c) rotates the M_2 FET by 90º eliminating the need for GSG contacts, thus only one gate finger used. This is possible because the M_2 transistor is not connected to ground. Here the width of M_2 must be doubled to maintain the same current density as the other designs. In the Figure 4.5(a,b) designs it is not possible to probe each transistor individually for characterization. The metal traces are too small for the typical 20 µm pitch DC probes. The Figure 4.5(c) design includes a minimum sized pad for this purpose. For all three redesigns the separation distance between the two FETs has been significantly reduced as compared to the initial layout. This results

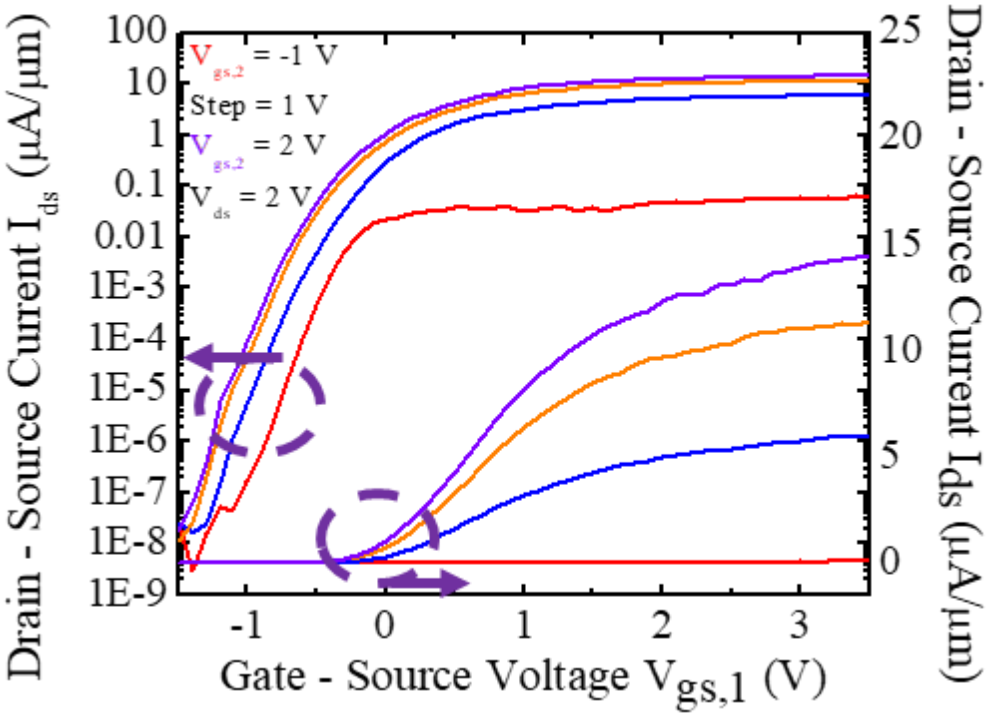

Figure 4.6: I_{ds}-$V_{gs,1}$ transfer curves for a CVD MoS_2 cascode. The left curves are in the log scale and the right curves are in the linear scale. The different traces are measured at different $V_{gs,2}$ bias points with a fixed V_{ds} = 2 V.

in the two FETs being composed of MoS_2 sheets which were grown in close vicinity, increasing the likelihood of better matched devices.

4.4 CVD MoS_2 Cascode DC Characterization

Figure 4.6 shows the I_{ds}-$V_{gs,1}$ transfer characteristics for a CVD MoS_2 cascode. This measured cascode data was taken using the Figure 4.5(c) design. The left curves are in the log scale while the right curves are in the linear scale. The family of curves represent different M_2 gate bias points, $V_{gs,2}$. This modulates the overall cascode current by changing the M_2 channel resistance. A sufficiently large drain bias, V_{ds} = 2 V, is applied to allow

headroom for both FETs to operate in saturation. At large $V_{gs,2}$ biases an I_{ON}/I_{OFF} ratio of 10^8 is observed, inheriting this same benefit of embedded gate FETs. From the linear curves, the extrapolated V_{ths} are close to 0 V, further confirming enhancement mode operation using embedded gates.

Figure 4.7(a) shows the I_{ds}-V_{ds} transfer curves for the same cascode. Here the same family of curves are sweeps at different M_2 biases, $V_{gs,2}$. The $V_{gs,1}$ bias is set sufficiently large to force M_1 on at all times. A similar set of curves can be obtained by holding the $V_{gs,2}$ bias high while sweeping V_{ds} at various $V_{gs,1}$ points. The output curves show saturating behavior exhibiting the improved output impedance of the cascode. Figure 4.7(b) is the same output curves measured for one of the cascode FETs, in this case the upper M_2 FET. Comparing a single FET to the cascode, the current density of the cascode is about half at the same drain bias. This is because the V_{ds} is dropped across two FETs applying a half V_{ds} to each FET. The separation of the curves at the maximum V_{ds} = 2 V is evenly spaced in the single FET while non-linear in the cascode. This is because the cascode FETs are not velocity saturated as the individual FETs operate closer to the triode (linear) region. The V_{ds} for each cascode FET is half the supply voltage so the channel electric fields are half.

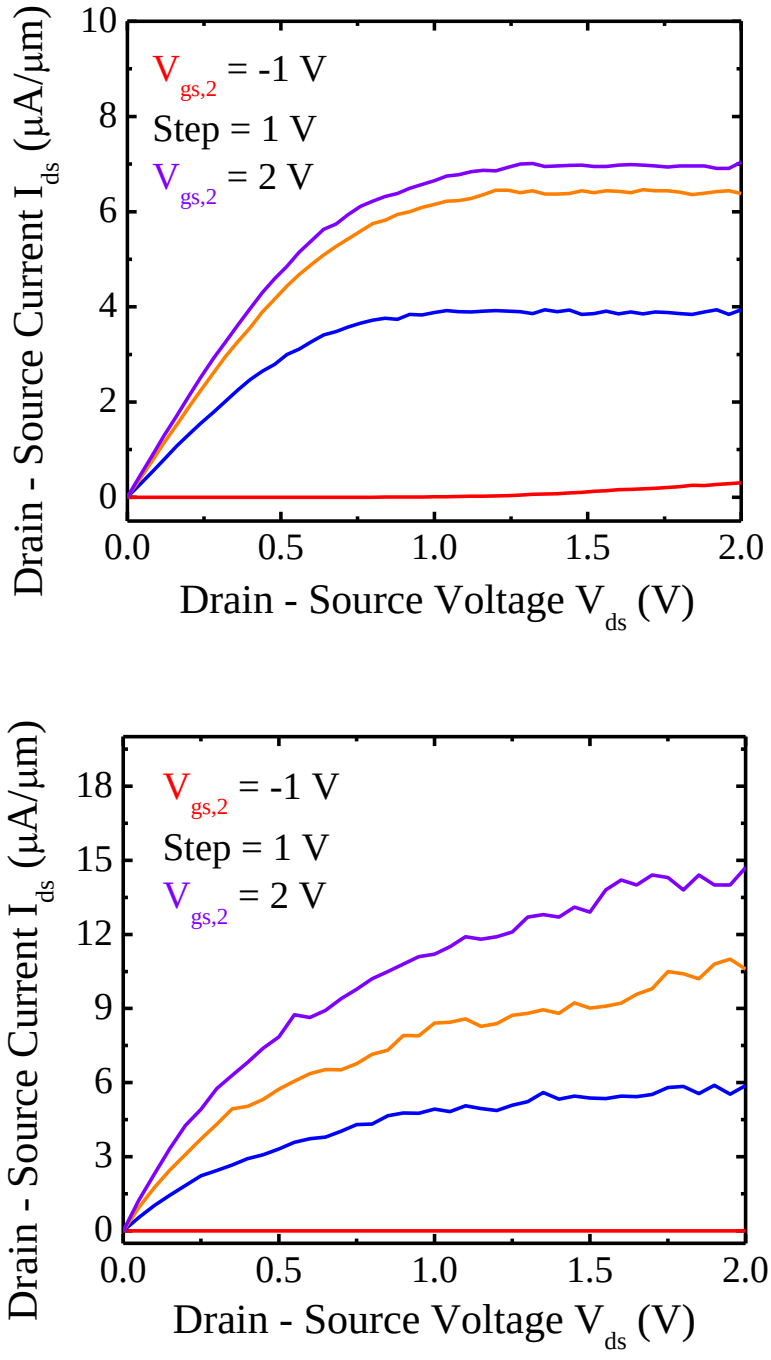

Figure 4.7: (a) I_{ds}-V_{ds} output curves for a MoS_2 cascode circuit. The $V_{gs,1}$ bias is held constant to maintain M_1 in saturation while V_{ds} is swept at various $V_{gs,2}$ points. (b) I_{ds}-V_{ds} output curves for a single FET within the same cascode circuit. In this case the upper M_2 FET is measured.

4.5 CVD MoS_2 Cascode RF Characterization

The DC characterization of CVD MoS_2 cascodes shows improved saturating characteristics as compared to a single FET. This increased output resistance, r_o, should improve the fmax of circuit, and in turn, the voltage gain of a cascode amplifier. The reduction of the Miller effect increases the cascode's bandwidth. Since the cascode was designed in the GSG configuration, the same high frequency measurement as taken for single FETs can be applied for the cascode. The only additional biasing required is the top cascode FET gate, which can applied with a DC probe since it is not in the high frequency path. The de-embedding of the cascode is not straightforward as the previous OPEN structure can only capture the parasitics of one FET. The middle node is floating in this scenario and will not be included in the OPEN. As a result additional studies into careful de-embedding of multi-FET GSG structures, are required. Here the high frequency extrinsic values are shown, which fully include the additional parasitics imposed by the cascode layout.

Figure 4.8(a) shows the h_{21} current gain vs. frequency for the CVD MoS_2 cascode. The blue line is a 20 dB/dec line which is used to extrapolate an extrinsic f_T of about 1 GHz. The f_T of a cascode is useful in that cascodes are often used in current sources. Figure 4.8(b) is the MAG vs. frequency for the same cascode. The f_{max} from this measurement is about 6 GHz, although the measurements have a large oscillation, indicating potential instability. In this cascode the fmax is six times the f_T, showing the increase in output resistance boosts the fmax in relation to the f_T. The ratio of f_{max} to f_T is larger in the cascode (based on embedded gate FETs) than the embedded gate FETs on chapter 3 and top-gated FETs of chapter 2. This highlights the advantage of cascading FETs in voltage and power

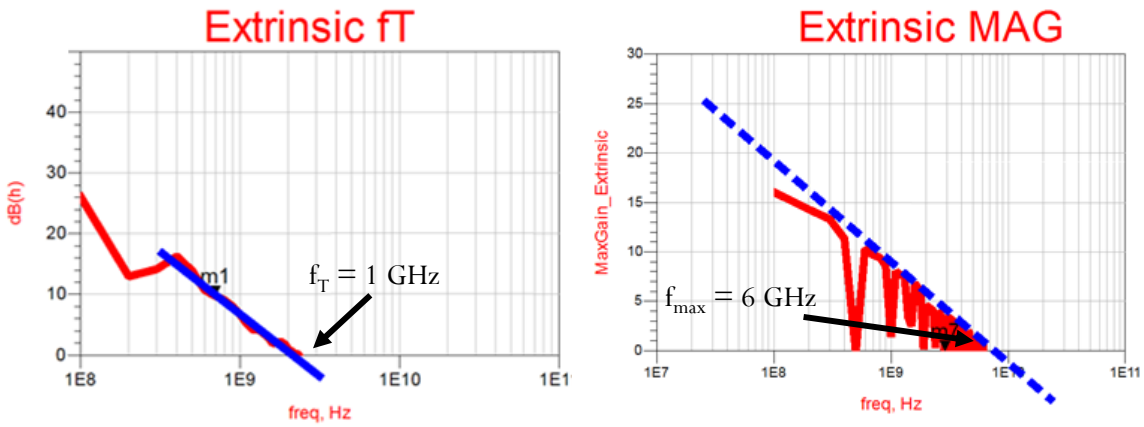

Figure 4.8: (a) Extrinsic h_{21} current gain vs. frequency for a CVD MoS_2 cascode. The transit frequency, f_T, is about 1 GHz. (b) Extrinsic maximum available gain, MAG, vs. frequency. The f_{max} is about 6 GHz. The blue lines are 20 dB/dec slopes.

amplifiers. Figure 4.9 shows the cascode f_T for different top transistor, $V_{gs,2}$ biases. In this scenario the top FET is acting as a variable resistor which modulates the overall cascode g_m. Going from the purple curve to the blue curve the f_T increases from about 500 MHz to 1 GHz, as the top transistor fully turns on.

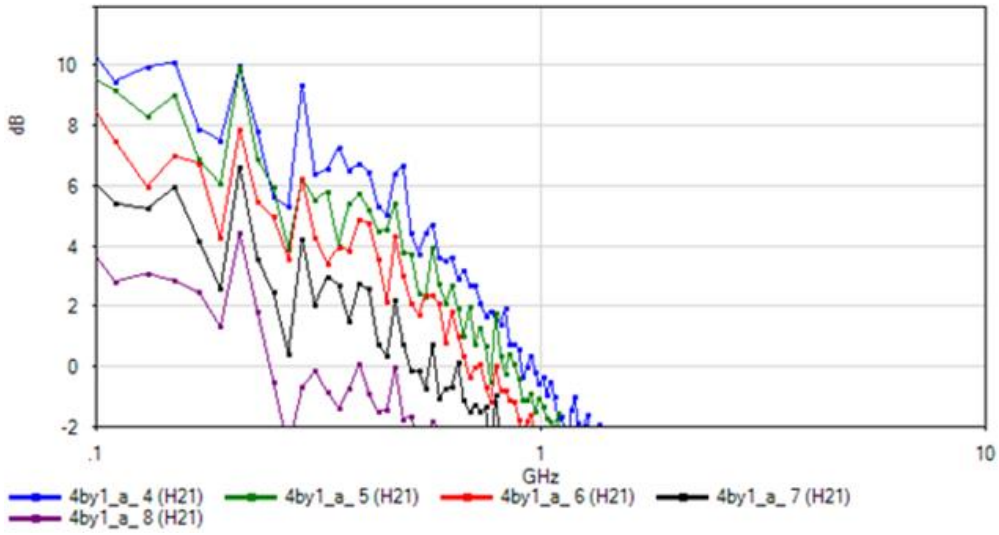

Figure 4.9: A CVD MoS_2 cascode extrinsic h_{21} current gain vs. frequency at different top FET gate biases, $V_{gs,2}$. The f_T increases from about 500 MHz to 1 GHz as $V_{gs,2}$ is increased from the purple to blue curve.

4.6 Summary

The motivation for making an embedded gate cascode circuit using CVD MoS_2 is to demonstrate the functionality of multiple integrated FETs. The simplest extension of the CVD MoS_2 common-source amplifier measured in chapter 2 is to put two FETs in series, creating a two-stage amplifier (cascode) commonly used in voltage and power amplifiers, and current sources. In order to perform high frequency measurements of the cascode, the layout was conformed to the GSG configuration. The initial design for the GSG cascode suffered from a large parasitic capacitance at the intermediate node between the two FETs. This caused a large roll off in gain, leading to a very low f_T in the MHz regime. To mitigate this parasitic capacitance, the cascode was redesigned with a minimal intermediate node metal area and sidewall length.

The DC characterization showed enhancement mode operation with an I_{ON}/I_{OFF} of 10^8, retaining the benefits of the embedded gate structure and gate-first process flow. The output curves showed that the cascode shows improved saturation, hence larger output resistance, compared with a single FET. The RF characterization of the redesigned CVD MoS_2 cascode yielded an extrinsic f_T and f_{max} of 1 and 6 GHz, respectively. The cascode f_{max}-to-f_T ratio is improved over the top-gated and single embedded gate due to the increased output resistance.

As shown with the common-source amplifier measurement in chapter 2, future development work for the CVD MoS_2 cascode includes performing a voltage amplifier measurement to observe the expected increase in the gain bandwidth product. The cascode simulations in chapter 3 included input and output matching networks for maximum power transfer. This can be experimentally included with integrated passives or wirebonding the MoS_2 cascode onto a designed PCB.

CHAPTER 5: CVD MoS_2 Dual-gated FETs

5.1 INTRODUCTION

Chapter 2 discussed CVD MoS_2 top-gated FETs and chapter 3 covered embedded gate FETs, highlighting the differences between the respective gate-last and gate-first devices. The major takeaway from this comparison is the observed difference in the interfacial doping effect of oxygen sub-stoichiometric oxide with MoS_2. The gate-first flow mitigates this effect by forming the MoS_2 interface with the last cycles of the ALD oxide process, which forms a much more stoichiometric interface. This resulted in the desirable positive V_{th}, for enhancement mode devices. Additionally, with embedded gates, the MoS_2-oxide interface has less organic contaminants and superior electrostatic gate control, leading to an improved mobility and I_{ON}/I_{OFF}. The disadvantage shown with the absence of the strong doping effect is a reduced current density, which is crucial in circuits driving large loads. One observation made in the embedded gate devices was that the top MoS_2 was exposed to ambient, allowing the application further passivation layers. More specifically, an oxygen deficient dielectric such as that used in the top-gated FETs may be applied to recover the lost current drive in the embedded gate FETs. Finally, the top dielectric can be independently or jointly gated with the embedded gate, creating a local dual-gated FET. A dual-gated FET is the next step towards a gate-all-around structure which maximizes the gate control of the MoS_2. An improved gating scheme is beneficial in suppressing short channel effects and improving the subthreshold slope of devices. This chapter discusses the design, fabrication, and electrical characterization of CVD MoS_2 dual-gated FETs.

5.2 DUAL-GATED MoS_2 RF FET FABRICATION

The derivation of the dual-gated FET fabrication flow is simplified in that it is combining the process flows of the previously outlined top-gated FET with the embedded gate FET. In other words, the fabrication of a dual-gated FET is an extension of the gate-first process flow, with an additional dielectric deposition and gate patterning/deposition [48]. It is possible to create separate contacts for each gate for independent biasing. The approach taken here is to electrically connect the two gates with a via. This dictates the two gates to be at the same applied voltage. Each gate contributes a different capacitance according to its dielectric layer thickness and composition. The minimum feature size 150 nm was kept for gate lengths, L_g, and the width, W, was maintained at 10 μm for convenient comparison with previous results.

Chapter one compared Al_2O_3 and HfO_2 dielectrics as a gate oxide for CVD MoS_2. The conclusion was that HfO_2 induces a much stronger doping effect, which improved current density and reduced contact resistance, at the cost of a large negative V_{th} shift and a few orders of I_{ON}/I_{OFF} reduction [49]. The Al_2O_3 dielectric did the opposite, however, its larger band gap allowed scaling its thickness down while maintaining low leakage currents. An ideal device takes advantage of both of these properties. With this goal in mind, the dual-gated FET was fabricated with an Al_2O_3 bottom dielectric and a HfO_2 top-dielectric. The dielectric thicknesses were set to match each gate oxide capacitance, such that each gate contributes equal current control capability. Figure 5.1 is a cross-sectional diagram of a MoS_2 dual-gated FET. The “eG” and “tG” labels are the embedded and top gates respectively. The thin light green layer is single layer CVD MoS_2 which is sandwiched by two gate dielectrics. Similar to the chapter 2 devices, a small top-gate underlap region was included to reduce its C_{gd} and C_{gs} overlap parasitic capacitance for RF consideration.

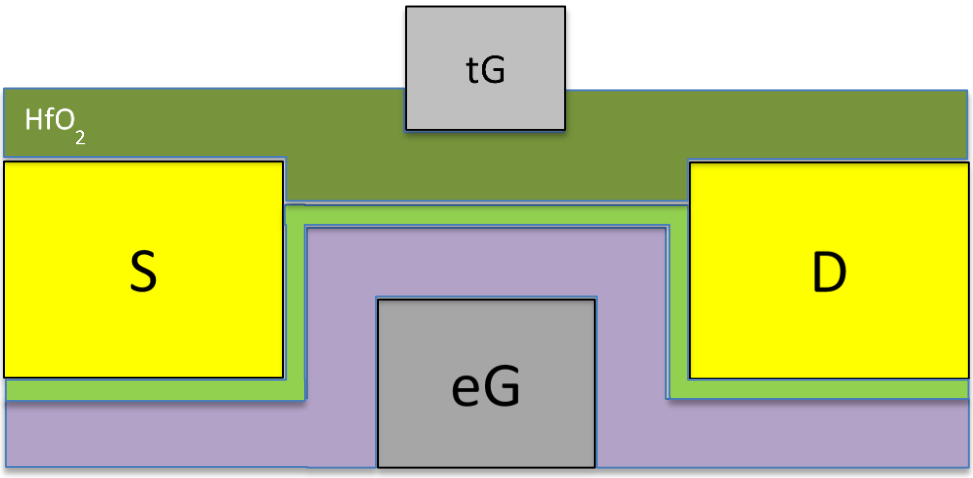

Figure 5.1: Cross-section of a dual-gated MoS_2 FET. The "eG" and "tG" labels are the embedded and top gates respectively. The bottom dielectric is Al_2O_3 and the top is HfO_2. The thin green layer is the single layer CVD MoS_2.

5.3 DUAL-GATED MoS_2 FET DC CHARACTERIZATION

The DC characterization highlights the advantages of the dual-gated configuration of MoS_2 FETs. Figure 5.2(a,b) shows the I_{ds}-V_{gs} transfer curves for two different MoS_2 dual-gated FETs. The red curves are for the embedded Al_2O_3-gated FETs without any additional top dielectric. The blue curve is the measurement immediately after the top dielectric HfO_2 ALD layer deposition. The black curve is the final dual-gated FET measurement. The red embedded gate FETs show enhancement mode operation with an I_{ON}/I_{OFF} of 10^7 (shown with the orange dashed arrow). After depositing sub-stoichiometric HfO_2 on the exposed top MoS_2, the devices incur a large negative V_{th} shift of about -3 V, as shown by the purple dashed arrow. The current measured at the maximum V_{gs} voltage point is improved by about an order of magnitude, increasing the I_{ON}/I_{OFF} to about 10^8, as indicated by the green dashed arrow. The black curve is dual-gated transfer curve, which is shifted back to the original V_{th} while maintaining the increased drive current. For the dual-gated measurement the V_{gs} voltage is applied to both gates at the same magnitude.

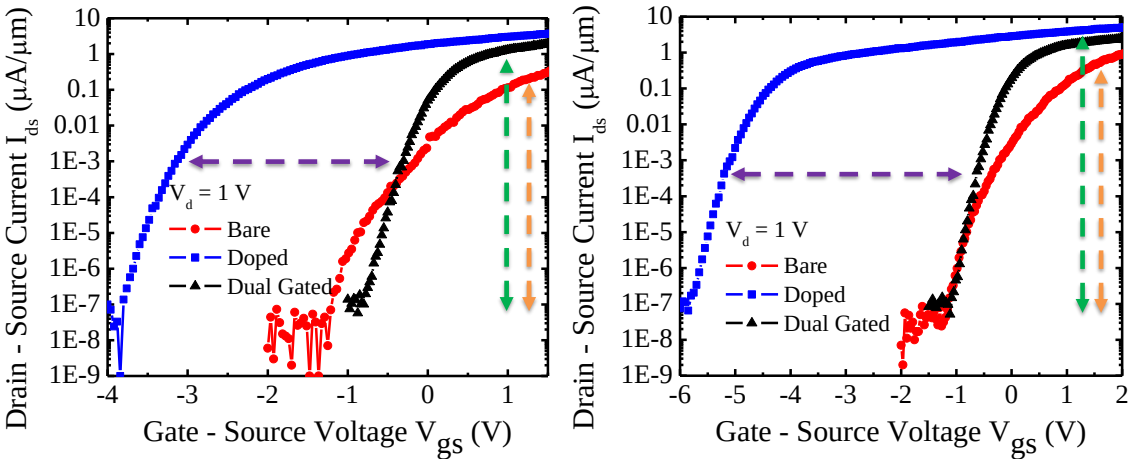

Figure 5.2: (a,b) Transfer curves, I_{ds}-V_{gs}, for two different dual-gated CVD MoS_2 FETs. The three curves compare embedded gate FETs (red), embedded gate FETs with a top dielectric (blue), and the final dual-gated FET (black). The purple horizontal arrow represents the V_{th} shift after the top dielectric HfO_2 doping. The orange and green vertical arrows show the I_{ON}/I_{OFF} improvement due to increased current drive.

The dual-gated FET improves the overall current density, I_{ON}/I_{OFF}, and subthreshold slope compared with the original embedded gate FET, all while maintaining the same V_{th}. The doped curve indicates a depleted mode device, which may implemented as is if desired. Additionally a more stoichiometric top dielectric layer such as Al_2O_3 may be used, which may sacrifice current density at the benefit of even further improve gate control. This highlights the flexibility of the dual-gated configuration.

Figure 5.3 is the transconductance, g_m, curves for an embedded gate FET, embedded gate FET with a top dielectric, and the final dual-gated FET. The maximum gm point follows the V_{th} shifts. The dual-gated maximum g_m is three times the original embedded gate FET. This is promising for using dual-gated FETs for RF devices where the f_T is proportional to g_m.

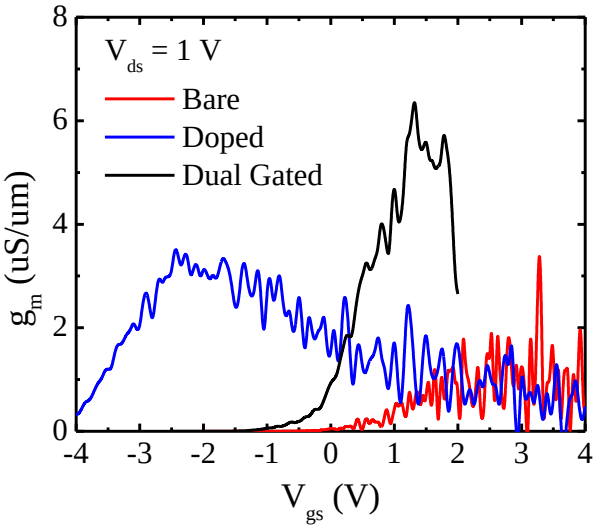

Figure 5.3: Transconductance, g_m, vs. gate voltage, V_{gs}, curves for a dual-gated CVD MoS_2 FET. The three curves compare an embedded gate FET (red), embedded gate FET with a top dielectric (blue), and the final dual-gated FET (black).

5.3.1 DIBL IN CVD MoS_2 FETS

Figure 5.3(a) show the dual-gate transfer curves at different drain biases, V_{ds}, while Figure 5.3(b) is the same embedded gate transfer curves as Figure 3.5(a). This figure compares the drain-induced barrier lowering (DIBL) present in the two devices. DIBL is a short channel effect where the drain bias affects the height of the source-to-channel barrier. The amount of DIBL present is determined by a fight between the gate-to-source and drain-to-source electrostatics. Short channel FETs may suffer from DIBL which manifests itself as a voltage shift in the subthreshold slope at different drain biases. The DIBL can be measured as $\frac{\Delta V_{th}}{\Delta V_{ds}}$ where a lower number indicates a suppressed effect. The dual-gated FETs should show a reduced DIBL due to the improved gate electrostatics. The Figure 5.3(a,b) comparison shows a dual-gated DIBL of 0.2 compared with an embedded gate value of about 0.3 when moving from a V_{ds} of 100 mV to 1 V. This represents a 33% improvement with the additional top-gate.

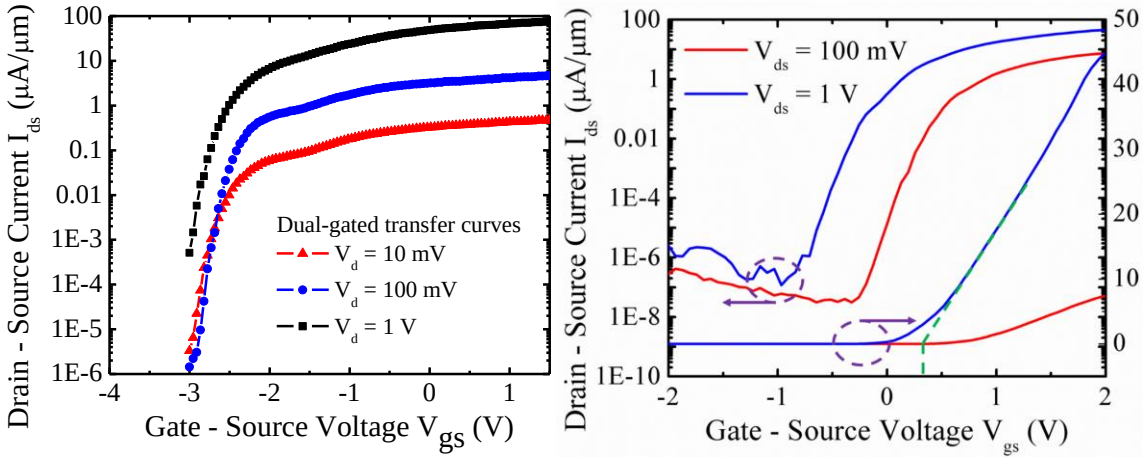

Figure 5.2: (a) Transfer curves for a dual-gated CVD MoS_2 FET at different drain biases V_{ds}. (b) Transfer curves for an embedded gate FET. This is the same as Figure 3.5(a). The two plots compare the degree of DIBL which is 0.2 in (a) and 0.3 in (b), when moving from a V_{ds} of 100 mV to 1 V.

5.4 Prospects of Dual-gated MoS_2 RF FETs

The DC characterization is promising for RF FETs in the improvement of g_m after dual gating. The expected RF performance requires a closer examination. The basic equation for f_T when operating in saturation is $f_T = \frac{g_m}{2\pi C_{gs}}$ where C_{gs} is the channel capacitance in saturation, $C_{gs} = \frac{2}{3}WLC_{ox}$. From the dual-gated configuration the C_{ox} doubles, assuming the same area for both gates. The g_m must at least double to expect the same f_T. Figure 5.3 showed a three times improvement in g_m which overcomes the accompanied C_{ox} increase. This dual gate design included underlap regions for the top gate. While this eliminates the direct overlap C_{gs} and C_{gd}, there are additional fringing components which contribute to the high frequency capacitance. The overall effect of f_T in a dual-gated MoS_2 FET warrants further study.

5.5 SUMMARY

Chapter 2 showed the results of high performance HfO_2 top-gated CVD MoS_2 FETs. These depletion mode FETs suffered from a large negative V_{th} shift due to the oxygen-deficient HfO_2 oxide interface, as well as organic contaminants on the MoS_2 surface. To mitigate this V_{th} shift, embedded gate FETs were studied in chapter 3. Embedded gate FETs took advantage of the gate-first process flow where the last cycles of ALD-grown Al_2O_3 oxide provide a stoichiometric and organic impurity-free interface upon which MoS_2 was transferred. These embedded gate FETs showed enhancement mode operation with improved I_{ON}/I_{OFF} and lower current densities as compared to their top-gated counterparts. The top MoS_2 was exposed to ambient in these devices, allowing for further passivation layers. In this chapter, a top HfO_2 oxygen-deficient top dielectric layer was applied to the embedded gate FET to improve the current densities. This induced an undesirable large negative V_{th} shift consistent with chapter 2's results. A top-gate was added to the device to help modulate the doping effect of the top dielectric. This created a CVD MoS_2 dual-gated FET which recovered the V_{th} back to the enhancement mode region of operation, while maintaining the improved current density, thus I_{ON}/I_{OFF}. The g_m of the dual-gated FETs showed a three times improvement compared with embedded gate FETs. The DIBL effect was suppressed by 33% due to the improved gate control afforded by dual gates. The f_T of dual-gated MoS_2 FETs may increase over embedded gate FETs in that its gm must improve by only more than double to exceed the doubling of C_{ox}. The high frequency performance of dual-gated MoS_2 RF FETs warrants further study.

Appendix

A.1 GSG DESIGN RULES AND RF MEASUREMENT SETUP

The measurement of high frequency devices is a challenge within itself. All of the external components and the DUT contribute parasitics which reduce the measurement bandwidth. In addition to the de-embedding procedure used to obtain intrinsic device characteristic, careful device layout and tool calibration is performed. The Cascade Infinity probes used for all high frequency measurements have a set of design rules to ensure compatibility. Figure A.1(a,b,c,) show a few of these design rules which dictate the layout of the MoS_2 RF FETs. Figure A.1(a) defines the minimum pad size and spacing. Figure A.1(b) gives a minimum GSG probe lateral spacing while Figure A.1(c) gives a minimum transverse spacing. Another consideration is the pitch size of the RF probes. This determines how far apart each GSG pad should be placed. All the measurements in this study used 100 μm pitch probes, however various probe sizes should not change the measured performance.

Another aspect to the RF measurement is the calibration of the test setup. This is accomplished with a short-open-load-thru (SOLT) calibration technique. The accuracy of

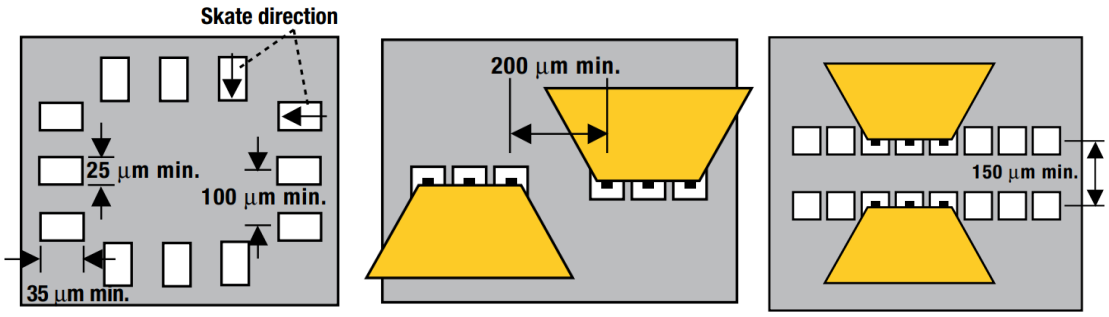

Figure A.1. (a) GSG minimum pad size and spacings. (b) Lateral space between GSG landing zones (c) GSG probe-to-probe minimum separation distance. Adapted from [50].

the SOLT procedure has a large impact upon the quality of the RF device measurement. Great care should be taken during this procedure in the bandwidth of interest. A few learnings from this exercise include minimizing the environmental interference with the test setup. One example is choosing an environment which has minimum vibrations, which contribute to the SOLT error. Repeated calibration cycles may be necessary when the SOLT does not produce satisfactory results. If the SOLT continues to produce unacceptable results, an open and thru frequency dependent measurement (as opposed to SOLT steps) on a sacrificial GSG pattern can give insight into whether DUT measurement is appropriate.

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